Study of macroscopic and microscopic homogeneity of DEPFET X-ray detectors

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Abstract

For the X-ray astronomy project Advanced Telescope for High ENergy Astrophysics (Athena) wafer-scale DEpleted P-channel Field Effect Transistor (DEPFET) detectors are proposed as Focal Plane Array (FPA) for the Wide Field Imager (WFI). Prototype structures with different pixel layouts, each consisting of 64 x 64 pixels, were fabricated to study four different DEPFET designs. This thesis reports on the results of the electrical and spectroscopic characterization of the different DEPFET designs. With the electrical qualification measurements the transistor properties of the DEPFET structures are investigated in order to determine whether the design intentions are reflected in the transistor characteristics. In addition, yield and homogeneity of the prototypes can be studied on die, wafer and batch level for further improvement of the production technology with regard to wafer-scale devices. These electrical characterization measurements prove to be a reliable tool to preselect the best detector dies for further integration into full detector systems. The spectroscopic measurements test the dynamic behavior of the designs as well as their spectroscopic performance. In addition, it is revealed how the transistor behavior translates into the detector performance. This thesis, as the first systematic study of different DEPFET designs on die and detector level, shows the limitations of the current DEPFET assessment methods. Thus, it suggests a new concise characterization procedure for DEPFET detectors as well as guidelines for expanded testing in order to increase the general knowledge of the DEPFET. With this study of four different DEPFET variants not only designs suitable for Athena mission have been found but also improvement impulses for the starting wafer-scale device production are provided.

Contents

Glossary

ADC	Analog to Digital Converter
APS	Active Pixel Sensor
ASIC	Application Specific Integrated Circuit
ASTEROID	Active current Switching Technique ReadOut In x-ray spectroscopy with DEPFET
Athena	Advanced Telescope for High ENergy Astrophysics
BOB	BreakOut Board
BP	Back Planes
C	Clear
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
CG	Clear Gate
CS	Complement Source
CuG	Cut Gate
D	Drain
DEPFET	DEpleted P-channel Field Effect Transistor
DIOS	Semiconductor process simulation software from SYNOPSYS
DR	Drain Readout
DWL	Direct Wafer Lithography
ENC	Equivalent Noise Charge
eROSITA	extended ROentgen Survey with an Imaging Telescope Array
ESA	European Space Agency
ESR	Extrapolation method of V_{Th} in the Saturation Region
FET	Field Effect Transistor
FWHM	Full Width Half Maximum
G	Gate
iG	internal Gate
InS	Inner Substrate
IS	Investigation Sensor
IXO	International X-ray Observatory

MIXS	Mercury Imaging X-ray Spectrometer
MOS	Metal Oxide Semiconductor
MUX	Keithley 3723 MUltipleXer-cards
NG	Narrow Gate
NMOS	N-channel Metal Oxide Semiconductor
OS	Outer Substrate
PCB	Printed Circuit Board
PMOS	P-channel Metal Oxide Semiconductor
QL	Quasi Linear
R1	Ring 1
ROAn	ROOT based Offline Analysis
S	Source
SF	Source Follower
SG	Short Gate
SMU	Keithley 2612A dual-channel Source Meter Unit
SRG	Spectrum-Roentgen-Gamma satellite
Switches	Keithley 3706-S system switch mainframes
TeSCA	Two-dimensional Semi-Conductor Analysis package of the Weierstrass-Institut fuer Angewandte Analysis und Stochastik
TOE	TOEllner power supply
VERITAS2.0	VErsatile Readout based on Integrated Trapezoidal Analog Shapers
WFI	Wide-Field Imager
X-IFU	X-ray Integral Field Unit
XMM-Newton	X-ray Multi-Mirror Mission
ZIF	Zero Insertion Force

List of Symbols

Symbol	Description	Unit
a	Amplitude of white noise	$\frac{\mathrm{V}^2}{\mathrm{Hz}}$
a_f	Amplitude of series $\frac{1}{f}$ noise	V^2
A_1	Weighting of white series noise of the filter	-
A_2	Weighting of $\frac{1}{f}$ noise of the filter	-
A_3	Weighting of white parallel noise of the filter	-
A_C	Cross section of the transistor channel	$\mu\mathrm{m}^2$
A_G	Gate area	$\mu\mathrm{m}^2$
A_CuG	Gate area of the cut gate DEPFET	$\mu\mathrm{m}^2$
A_NG	Gate area of the narrow gate DEPFET	$\mu\mathrm{m}^2$
A_QL	Gate area of the quasi linear DEPFET	$\mu\mathrm{m}^2$
A_SG	Gate area of the short gate DEPFET	$\mu\mathrm{m}^2$
b	Amplitude of leakage noise	$\frac{\mathrm{C}^2}{\mathrm{s}}$
C_Det	Effective detector input capacitance	F
C_G	Gate capacitance	F
C'_G	Gate capacitance per unit area	$\frac{\mathrm{F}}{\mathrm{m}^2}$
C_Ni	Gate nitride capacitance	F
C_Ox	Gate oxide capacitance	F
d	Device thickness	$\mu\mathrm{m}$
d_C	Transistor channel thickness	$\mu\mathrm{m}$
d_Ox	Gate oxide thickness	$\mu\mathrm{m}$
d_Ni	Gate nitride thickness	$\mu\mathrm{m}$
$\mathcal{E}$	Electric field	$\frac{\mathrm{V}}{\mathrm{m}}$
E_C	Energy level of the conduction niveau	eV
$E_{\mathrm{e^-h^+}}$	Generation energy of $\mathrm{e^-h^+}$ pairs for silicon = 3.68	$\frac{\mathrm{eV}}{e^-}$
E_F	Energy level of the fermi niveau	eV
E_Fm	Energy level of the fermi niveau for metals	eV

Symbol	Description	Unit
E_{Fn}	Energy level of the fermi niveau for n doped silicon	eV
E_{Fp}	Energy level of the fermi niveau for p doped silicon	eV
E_{i}	Intrinsic energy level	eV
E_{Photon}	Energy of the absorbed photon	eV
E_{V}	Energy level of the valence niveau	eV
E_{Vacuum}	Energy level of the vacuum niveau	eV
ENC_{Filter}	ENC of the filter	e^- rms
ENC_{Theo}	Reachable ENC in theory	e^- rms
ENC_{Meas}	Measured ENC	e^- rms
f_{Fano}	Fano factor of silicon = 0.117	-
$Fano$	Fano noise	e^- rms
$FWHM_{\mathrm{Theo}}$	Reachable FWHM in theory	eV
$FWHM_{\mathrm{Meas}}$	Measured FWHM	eV
g_{Asteroid}	Asteroid gain	$\frac{\mathrm{ADU}}{\mathrm{V}}$
g_{d}	Detector gain	$\frac{\mu\mathrm{V}}{e^-}$
g_{C}	Slope of $5 \cdot 10^{-6}$ in the clear characteristics for the defined onset of the clear	$\frac{\mathrm{A}}{\mathrm{V}}$
g_{C64}	Slope of $2 \cdot 10^{-5}$ in the column wise clear characteristics for the defined onset of the clear	$\frac{\mathrm{A}}{\mathrm{V}}$
g_{CG}	Slope of $5 \cdot 10^{-6}$ in the clear gate characteristics for the defined onset of the clear gate	$\frac{\mathrm{A}}{\mathrm{V}}$
g_{CG64}	Slope of $2 \cdot 10^{-5}$ in the column wise clear gate characteristics for the defined onset of the clear gate	$\frac{\mathrm{A}}{\mathrm{V}}$
g_{q}	Charge transconductance	$\frac{\mathrm{pA}}{e^-}$
g_{m}	FET transconductance	$\frac{\mathrm{A}}{\mathrm{V}}$
g_0	FET output conductance	$\frac{\mathrm{A}}{\mathrm{V}}$
g_{m64}	Transconductance of one matrix column for V_{On64} and I_{On}	$\frac{\mathrm{A}}{\mathrm{V}}$
$Gain_{\mathrm{Meas}}$	Measured system gain including DEPFET, Asteroid and buffer	$\frac{\mathrm{ADU}}{\mathrm{eV}}$
I_{Leak}	Leakage current	$\frac{e^-}{\mu\mathrm{s} \cdot \mathrm{pixel}}$
I_{PMOS}	Transistor current	μA
I_{On}	Transistor current of 100 μA that is defined as the on-state of the transistor	μA

Symbol	Description	Unit
k	Boltzmann's constant $= 1.38 \cdot 10^{-23}$	$\frac{\mathrm{J}}{\mathrm{K}}$
L	Gate length	µm
m	Slope of the source potential during V_{Gon} variation	-
N	Number of electron-hole pairs	-
N_{A}	Acceptor concentration	$\frac{1}{\mathrm{cm}^3}$
N_{D}	Donor concentration	$\frac{1}{\mathrm{cm}^3}$
N_{Leak}	Noise from leakage current	e^- rms
P_2B	Peak to background of all valid events	-
q	Magnitude of electronic charge $= 1.602 \cdot 10^{-19}$	As
Q'_0	Effective interface charge per unit area	$\frac{\mathrm{C}}{\mathrm{cm}^2}$
$Q'_{\mathrm{C}}(y)$	Channel charge per unit area	$\frac{\mathrm{C}}{\mathrm{cm}^2}$
$Q'_{\mathrm{D}}(y)$	Depletion region charge per unit area	$\frac{\mathrm{C}}{\mathrm{cm}^2}$
$Q'_{\mathrm{G}}(y)$	Gate charge per unit area	$\frac{\mathrm{C}}{\mathrm{cm}^2}$
$Q'_{\mathrm{I}}(y)$	Inversion layer charge per unit area	$\frac{\mathrm{C}}{\mathrm{cm}^2}$
Q_{iG}	Charge collected in the internal gate	C
t_{Clear}	Clear time	ns
t_{Frame}	Frame time	ns
t_{Int}	Integration time or charge accumulation time	ns
t_{Muxout}	Multiplexing time	ns
t_{Overlap}	Overlap time between clear and clear gate on-state	ns
t_{Read}	Readout time	ns
t_{Row}	Processing time for one row	ns
t_{Settle}	Settling time	ns
T_{Meas}	Measurement temperature	°C
v_{P}	Hole velocity	$\frac{\mathrm{m}}{\mathrm{s}}$
V_{B}	Backside voltage	V
V_{C}	Clear voltage	V

Symbol	Description	Unit
V_{CB}	Voltage drop between channel element and bulk	V
V_{CG}	Clear gate voltage	V
V_{CGoff}	Clear gate off voltage	V
V_{CGon}	Clear gate on voltage	V
V_{CGonset}	Clear gate voltage for the onset of the complete clear	V
$V_{\mathrm{CGonset64}}$	Clear gate voltage for the onset of the complete clear for 64 transistors of one column in parallel	V
V_{Coff}	Clear off voltage	V
V_{ComG}	Complement gate voltage	V
V_{ComS}	Complement source voltage	V
V_{Con}	Clear on voltage	V
V_{Conset}	Clear voltage for the onset of the complete clear	V
V_{Conset64}	Clear voltage for the onset of the complete clear for 64 transistors of one column in parallel	V
V_{CS}	Voltage drop between channel element and source	V
V_{D}	Drain voltage	V
V_{DS}	Voltage drop between drain and source	V
$V_{\mathrm{DS,sat}}$	Saturation voltage between drain and source	V
V_{Early}	Early voltage	V
V_{F}	Front side voltage	V
V_{FB}	Flatband voltage	V
V_{G}	Gate voltage	V
V_{GB}	Voltage drop between gate and bulk	V
V_{Goff}	Gate off voltage	V
V_{Gon}	Gate on voltage	V
V_{GS}	Voltage drop between gate and source	V
V_{InS}	Inner substrate voltage	V
V_{On}	Gate voltage for the on-state of the PMOS transistors that is reached when 100 µA flow through one pixel	V
V_{On64}	Gate voltage for the on-state of the 64 PMOS transistors in one column that is reached when 300 µA flow through one column	V
V_{R1}	Ring voltage	V
V_{S}	Source voltage	V
V_{SB}	Voltage drop between source and bulk	V
V_{Th}	Threshold voltage	V

Symbol	Description	Unit
V_{Th64}	Threshold voltage of one column (64 transistors)	V
W	Gate width	µm
X_{Si}	Electron affinity of silicon = 4.05	V
α	Length parameter of the filter weighting function	-
β	Transistor characteristic constant	$\frac{\mu A}{V^2}$
$\beta_{\mathrm{fit,lin}}$	Transistor characteristic constant fitted in the linear region of the output characteristics	$\frac{\mu A}{V^2}$
$\beta_{\mathrm{fit,sat}}$	Transistor characteristic constant fitted in the saturation region of the output characteristics	$\frac{\mu A}{V^2}$
$\beta_{\mathrm{SG,theo}}$	Theoretical transistor characteristic constant of the short gate device	$\frac{\mu A}{V^2}$
Δ_{Die}	Full width of a measured parameter per die	-
ϵ_0	Permittivity of free space = $8.854 \cdot 10^{-12}$	$\frac{As}{Vm}$
ϵ_{Ni}	Permittivity of nitride = 7	-
ϵ_{Ox}	Permittivity of silicon oxide = 3.9	-
ϵ_{Si}	Permittivity of silicon = 11.9	-
λ	Channel length modulation parameter	$\frac{1}{V}$
μ_{P}	Charge carrier mobility	$\frac{m^2}{Vs}$
ρ	Charge density per volume	$\frac{As}{m^3}$
σ	Standard deviation	-
τ	Shaping time or effective measurement time of the weighting function	µs
τ_{BP}	Delay time after changing multiplexer-to-backplane connections	s
τ_{MUX}	Delay time after closing or opening channels of the multiplexer cards	s

Symbol	Description	Unit
τ_{SMU}	Delay time after changing applied voltages with the source meter unit	s
Φ	Electrostatic potential	V
Φ_{bi}	Built-in potential on a pn junction	V
Φ_{F}	Fermi potential	V
Φ_{MS}	Contact potential between metal and semiconductor	V
Φ_{Ox}	Oxide charge potential	V
Φ_{WM}	Work function potential of metal	V
Φ_{Sn}	Work function potential of n doped silicon	V

1. Introduction

Silicon-based detectors are used today in many fields of science and technology. A significant share of these detectors are used for X-ray detection. Commonly known detector concepts are the diode strip detector, the drift detector and the Charge Coupled Device (CCD) [1]. These solid state devices are based on the principle of separating an electron-hole pair cloud produced by the interaction of ionizing radiation or particles with absorbing matter. The X-ray detectors are i.a. applied in medicine, material testing, particle physics, photon science and X-ray astronomy.

To observe cosmic X-rays, a balloon experiment or satellite is needed because the X-ray photons are shielded by the earth's atmosphere. With the rapidly evolving satellite and detector technology, the fascinating structures of the universe become bit by bit observable. From one X-ray mission to the next the grasp of the mirrors (product of effective area and field of view) as well as time and energy resolution increase. From X-ray Multi-Mirror Mission (XMM-Newton) [2, 3] launched in 1999, to extended ROentgen Survey with an Imaging Telescope Array (eROSITA) on board of the Spectrum-Roentgen-Gamma satellite (SRG) [4, 5] launching in 2016, for instance, the field of view as well as the grasp is quadruplicated at photon energies of 1 keV [4].

Recently the European Space Agency (ESA) approved a new X-ray mission called Advanced Telescope for High ENergy Astrophysics (Athena) [6] for selection as their next large mission with a launch foreseen in 2028. With Athena[1], major questions of astrophysics will be addressed like how large scale structures of the universe assemble and how black holes shape the universe. Understanding of these issues can be obtained by observing X-rays emitted by hot gases and black holes in high spectral resolution. For this purpose, better observational capabilities of angular and spectral resolution, detection sensitivity and throughput must be provided.

Therefore, Athena will be furnished with an X-ray telescope based on ESA's silicon pore optics combined with two scientific instruments, see table 1.0.1. The two instruments fulfill the complementary tasks of first finding and pre-characterizing the objects discovered by pathfinder missions like e.g. eROSITA in the 0.2 - 15 keV band with a wide field of view, and then do a full characterization with extremely high spectral resolution for the objects of interest. The Active Pixel Sensor (APS) of the Wide-Field Imager (WFI) provides a field of view of approx. $40\,'$ and a spectroscopic resolution close to the Fano limit. The micro-calorimeter of the X-ray Integral Field Unit (X-IFU) utilizing Transition Edge Sensors will perform spatially resolved high resolution X-ray spectroscopy in a field of view of approx. $5\,'$.

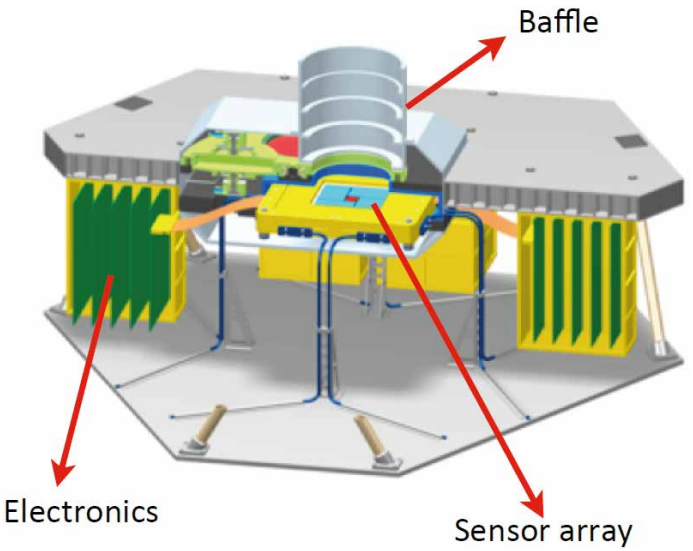
[1] see `http://www.the-athena-x-ray-observatory.eu/` or `http://sci.esa.int/cosmic-vision/54517-athena/` for more information

	Wide-Field Imager (WFI)	X-ray Integral Field Unit (X-IFU)
Effective area of the Silicon Pore Optic	2 m^2 @ 1 keV 0.25 m^2 @ 6 keV	
Angular resolution	5 ″ on-axis 10 ″ @ 25 ′ radius	
Field of view	40 ′	5 ′
Energy range	0.2 - 12 keV	
Spectral resolution	$<$ 150 eV @ 6 keV	$<$ 2.5 eV @ 6 keV

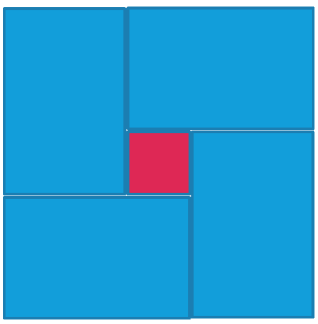
Table 1.0.1.: Requirements of the instruments for Athena mission [6].

ATHENA's WFI will be the main responsibility of the Max-Planck-Institute for extraterrestrial physics and the scientific goals of this thesis belong within the scope of this project. A concept drawing of the WFI is shown in figure 1.0.1a. The focal plane array of the WFI is depicted in figure 1.0.1b. It is currently [2] foreseen to consist of five DEpleted P-channel Field Effect Transistor (DEPFET) APS: four outer detector devices with 448 × 640 pixels of 130 µm × 130 µm pixel area and one 256 × 256 device of 100 µm × 100 µm pixels with a built-in shutter and intermediate storage.

[2] It is referred to the WFI concept from the White Paper 2014 [6]. The instrument design might change throughout the development phases.



(a) Design drawing of the WFI.



(b) Layout of the WFI focal plane array.

Figure 1.0.1.: Design drawing of the WFI [6] and the layout of the WFI focal plane array consisting of five DEPFET Active Pixel Sensors: four 448 × 640 matrices (blue) and one 256 × 256 matrix with a built-in shutter and intermediate storage (red) [7].

The DEPFET is a semiconductor APS with internal amplification optimized for X-ray detection, which was proposed by Kemmer and Lutz in 1987 [8]. Since then the DEPFET has developed into a detector concept successfully used in a variety of applications, e.g. the Mercury Imaging X-ray Spectrometer (MIXS) on BepiColombo mission [9], and it is proposed for a number of future projects in photon science [10], high energy particle physics [11] as well as for space applications [12].

As will be pointed out more in detail in chapter 2, DEPFET detectors are well suited for Athena because:

- they provide an excellent energy resolution of less than 130 eV @ 6 keV, as shown previously [13, 14]. This is close to the Fano limit, which is the fundamental limit for the spectral resolution in photon detection.
- they can be read out fast with low noise. The noise can be even decreased further by using special designs investigated in [15, 16].
- they can be accessed flexibly, row-wise, pixel-wise or in a flexible window mode.
- they can be easily adapted to the resolution of the X-ray optics by scaling the pixel size with drift rings used in [9, 17, 18].
- pixel arrays can be formed in various sizes, as has been proven in [9, 13].
- they show good radiation tolerance. Unlike a CCD, for example, no charge transfer is needed. Details can be found in [19, 20].

In order to reach the field of view of approx. 40 $'$ for Athena, wafer-scale DEPFET detectors with 448 $\times$ 640 pixel will be needed. The DEPFET production is elaborate and expensive owing to double sided processing as they are backside illuminated devices and require special care for the entrance window treatment. In total, the production requires over all 10 implantation and 19 thermal steps. The DEPFET devices are single defect sensitive for short-circuits making extensive manual inspection procedures for the 8 deposition and 7 structure etching steps necessary. The goal of this thesis is to provide technology and design learning to support the achievement of the needed high device yield and homogeneity for Athena.

The DEPFET functional principle and scientific concept are presented in chapter 2. The DEPFET matrices investigated in this thesis are prototypes with 64 $\times$ 64 pixel of 100 µm $\times$ 100 µm and are referred to as Investigation Sensor (IS). The IS have been produced in the scope of International X-ray Observatory (IXO) [12] and Athena to study the impact of various design parameters by detailed investigation of four different variations. The impact of the device type on typical parameters like spectral performance, operational parameters and internal amplification is examined. The devices with the different designs were distributed over the entire wafer area for homogeneity and yield studies, as shown in section 2.3.

All prototypes have been characterized electrically to provide homogeneity and yield learning on die, wafer and batch level. The electrical characterization and the used measurement setup are presented in chapter 3. For every DEPFET design, a defect

free pre-characterized detector die is integrated into a full detector system. The design properties determined by the electrical characterization will translate into the performance of the detector and its operational parameters. The performed spectroscopic measurements as well as the used setup are presented in chapter 4. To conclude the thesis, the results of both measurements are used to define a concise characterization procedure as well as to assess the design variants with respect to the high requirements of Athena in chapter 5.

2. DEPFET concept

This chapter introduces the DEPFETs Active Pixel Sensor (APS) concept. It starts with an overview of the interaction of photons and semiconductors. Afterwards the DEPFET structure is presented including the model commonly used to provide an understanding of the device. It also shows the most common way to form matrices out of the DEPFET pixels. Finally an overview of the four DEPFET design variants studied in this thesis is given.

2.1. Interaction of photon and semiconductor

There are four ways of interaction between photons and matter: reflection, transmission, absorption and scattering. Within the scope of this work, only the photo absorption of X-ray photons in silicon is regarded as it is with over 90% the most probable interaction in the energy band of 0.1 keV to 15 keV. As mentioned in chapter 1, Athena aims at spatially resolved spectroscopy of hot gases and black holes and one way to measure the energy of an X-ray photon of astrophysical origin is to absorb and detect all its energy in a detector. A more detailed description of other interaction mechanisms, like Rayleigh and Compton scattering in the X-ray band, is given e.g. in [21].

Assuming the absorption of one X-ray photon with the energy E_{Photon} in a fully depleted silicon bulk, the average number N of electron-hole pairs generated is given by

$$N = \frac{E_{\mathrm{Photon}}}{E_{\mathrm{e^-h^+}}} \tag{2.1.1}$$

Using the mean electron-hole pair creation energy $E_{\mathrm{e^-h^+}} = 3.68$ eV from [22] and $E_{\mathrm{Photon}} = 5895$ eV of the Mn-Kα_{1+2} line [23] typically emitted from a ^{55}Fe calibration source, results in an average number of electron-hole pairs of

$$N = \frac{5895\ \mathrm{eV}}{3.68\ \mathrm{eV}} = 1602 \tag{2.1.2}$$

So far, only the average of generated electron-hole pairs N was considered. But the probability for the production of the same number of electron-hole pairs by photons with the same E_{Photon} is not constant. Within the absorption process a varying amount of energy can also be transferred to the silicon lattice. The probability distribution has a Gaussian shape with a deviation described by the phenomenological factor f_{Fano}, the so-called Fano factor [24]. Multiplying equation 2.1.1 by this factor, gives the Fano noise

$$Fano = \sqrt{\frac{E_{\mathrm{Photon}}}{E_{\mathrm{e\text{-}h+}}} \cdot f_{\mathrm{Fano}}} \tag{2.1.3}$$

In spectroscopy, the spectral resolution is usually described as Full Width Half Maximum (FWHM) of the ideally Gaussian shaped peaks

$$FWHM = 2\sqrt{2ln2} \cdot E_{\text{e-h+}} \cdot \sqrt{Fano^2} \approx 2.355 \cdot E_{\text{e-h+}} \cdot \sqrt{Fano^2} \tag{2.1.4}$$

The best achievable spectral resolution for the detection of a Mn-Kα_{1+2} line can be calculated using

$$FWHM = 2.355 \cdot 3.68 \text{ eV} \cdot \sqrt{13.7^2} = 119 \text{ eV} \tag{2.1.5}$$

with f_{Fano} =0.117 for silicon taken from [22]. In Addition, the influence of readout noise and leakage current must be considered. The latter is treated differently for integrating detectors and time-continuous readout detectors, as will be explained later in section 2.2.5.

2.2. The DEPFETs functional principle

In the WFI the X-rays are planned to be detected using DEPFET APS arrays. In essence, the DEPFET is a combination of two Field Effect Transistor (FET) structures on a fully depleted bulk. As will be explained in this section, it is used to detect the ionizing radiation with the principle of charge separation.

2.2.1. DEPFET structure

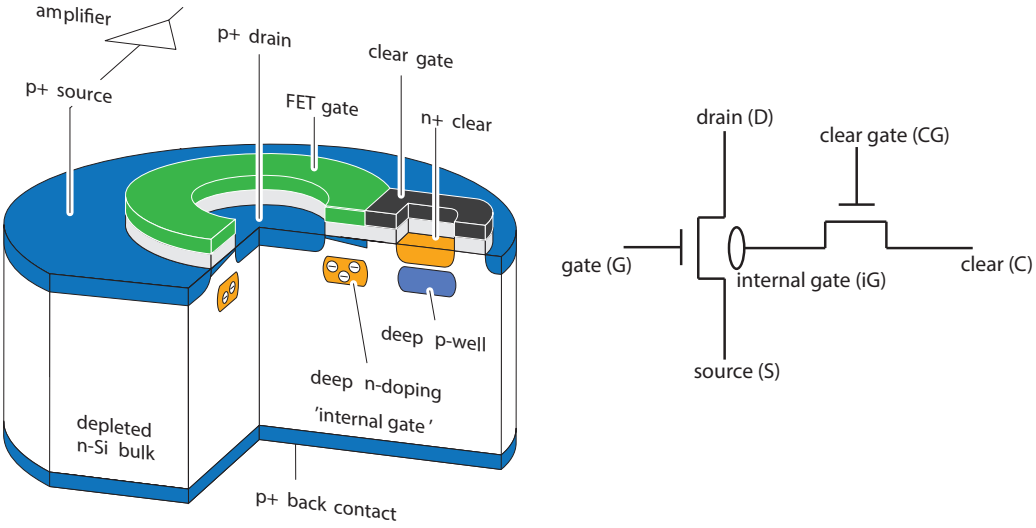


Figure 2.2.1.: The schematic drawing of a DEPFET structure displays the circular PMOS transistor and the adjoining clear transistor. It also gives a sectional view of the internal gate (iG) and the clear (C) contact with deep p-well shielding towards the bulk (adapted from [25]). Electrically, the DEPFET can be outlined using the depicted equivalent circuit diagram.

The circular cutaway and the equivalent circuit of the DEPFET are shown in figure 2.2.1. A DEPFET consists of two transistors: A P-channel Metal Oxide Semiconductor (PMOS) enhancement-mode transistor is formed by the p+ doped drain

and source contacts on n-silicon bulk and the external Metal Oxide Semiconductor (MOS) gate. A N-channel Metal Oxide Semiconductor (NMOS) transistor is formed by the n-doped region below the gate, the voltage controllable barrier called clear gate and the n+ doped clear contact, which is shielded towards the bulk by a p-implanted well. Before the operation of the combination of these two transistors is explained, the function of a single transistor is deduced from electronic basic concepts following standard literature like [26, 27, 28, 29, 30, 31].

2.2.2. Transistor characteristics

In the following, the transistor current characteristics is derived for a linear PMOS transistor as shown in figure 2.2.2. The transistor is composed of the gate MOS structure and two pn junctions for source and drain. For simplicity, these two terminals are regarded separately at first. The gate length L is defined along the y coordinate and the gate width W along z. The positive x coordinate points from the gate to the backside of the bulk.

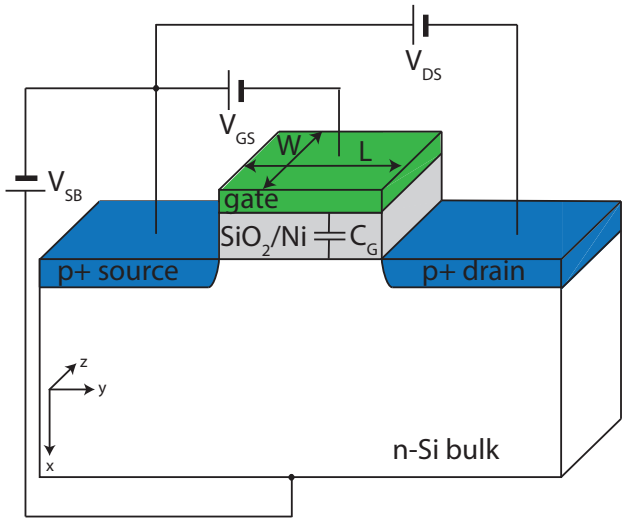


Figure 2.2.2.: PMOS transistor schematic including drain (D), source (S) and gate (G) on n-doped silicon bulk. The gate (G) consists of metal on top of nitride (Ni) and silicon oxide (SiO_2) acting as insulator. The gate length L is defined along the y coordinate and the gate width W along z.

Gate MOS structure

The gate is the voltage controllable barrier of the transistor that controls the electrical connection between drain and source. The MOS structure depicted in figure 2.2.3 is placed on a n-doped silicon bulk. Doped means, that pure silicon is intentionally introduced with impurities. To produce n-doped semiconductors, donor ions with five valence electrons like e.g. phosphor or arsenic are implanted. In contrary for p-doped silicon, acceptor ions with three valence electrons like e.g. boron are used. The bulk doping N_D is considered constant. As a consequence of the added donor atoms, electrons are the majority and holes the minority charge carrier. The MOS layers

can be approximated as series of parallel plate capacitors of the oxide and nitride layers with C_{Ox} and C_{Ni} as indicated in figure 2.2.3 that form the gate capacitance C_{G}

$$\frac{1}{C_{\mathrm{G}}} = \frac{1}{C_{\mathrm{Ox}}} + \frac{1}{C_{\mathrm{Ni}}} \tag{2.2.1}$$

with

$$C_{\mathrm{Ox}} = \epsilon_{\mathrm{Ox}} \cdot \epsilon_0 \cdot \frac{A}{d_{\mathrm{Ox}}} \tag{2.2.2}$$

and respectively for C_{Ni}

$$C_{\mathrm{Ni}} = \epsilon_{\mathrm{Ni}} \cdot \epsilon_0 \cdot \frac{A}{d_{\mathrm{Ni}}} \tag{2.2.3}$$

Inserting the permittivity of free space ϵ_0, the permittivity of nitride $\epsilon_{\mathrm{Ni}} = 7$ [32], the permittivity of silicon oxide $\epsilon_{\mathrm{Ox}} = 3.9$ [31] as well as the layer thickness $d_{\mathrm{Ni}} = 30$ nm and $d_{\mathrm{Ox}} = 180$ nm results in a gate capacitance per unit area C'_{G} of

$$C'_{\mathrm{G}} = 1.76 \cdot 10^{-4} \ \frac{\mathrm{F}}{\mathrm{m}^2} \tag{2.2.4}$$

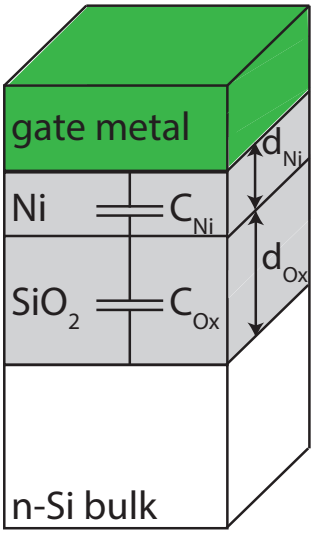
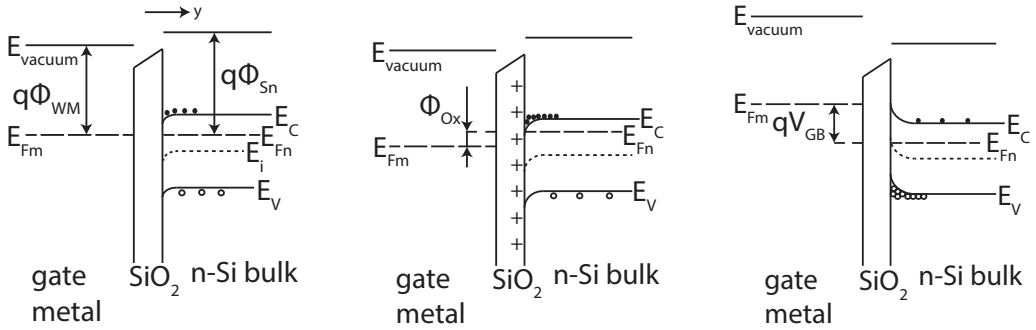


Figure 2.2.3.: The gate MOS structure can be approximated as capacitor.

Depending on the applied gate voltage, charge will accumulate at the metal-nitride interface and the counter charge at the silicon oxide-bulk interface. To enable an electrical connection, and thus a current I_{PMOS} between p+ doped source and drain of the transistor, holes must be accumulated below the gate. The current path underneath the MOS gate is called transistor channel. In order to understand how the minority charge carriers are accumulated in the channel, a closer look on the band structure is necessary.



(a) Without external bias. $\Phi_{\mathrm{WM}} < \Phi_{\mathrm{Sn}}$

(b) Without external bias but under consideration of existing oxide charge.

(c) With external gate bias to ensure inversion.

Figure 2.2.4.: Band structure of the metal oxide semiconductor. Dots on the conduction band E_{C} symbolize electrons and the circles below the valence band E_{V} holes.

Figure 2.2.4 schematically depicts a band structure of the MOS assuming that the work function potential (E_{Vacuum}-E_{F}) of the semiconductor bulk Φ_{Sn} is greater than that of the gate metal Φ_{WM} for three cases:

1. In absence of an external voltage, see figure 2.2.4a: Due to the work function potential difference $\Phi_{\text{WM}} < \Phi_{\text{Sn}}$, the conduction E_{C}, intrinsic E_{i} and valence band E_{V} of the semiconductor are bent downward. The Fermi level of the n-Si bulk E_{Fn} and the metal E_{Fm} are at the same energy level.

2. With added oxide charge potential Φ_{Ox}, which exists at every interface between silicon and silicon oxide, see figure 2.2.4b: The additional charge leads to an attraction of majority charge carrier, namely electrons, on the semiconductor oxide interface. The effect can be increased by applying a positive voltage to the gate. The gathering of majority charge carrier is also called accumulation.

3. With negative external gate bias V_{GB}, see figure 2.2.4c: The energy bands of the semiconductor are bent upward. Thus, holes will accumulate underneath the gate, if the negative bias overcomes the natural bending due to the contact potential $\Phi_{\text{MS}} = \Phi_{\text{WM}} - \Phi_{\text{Sn}}$ and the oxide charge potential Φ_{Ox}. The state, when more holes (minority charge carrier) than electrons (majority charge carrier) are located below the gate, is called inversion.

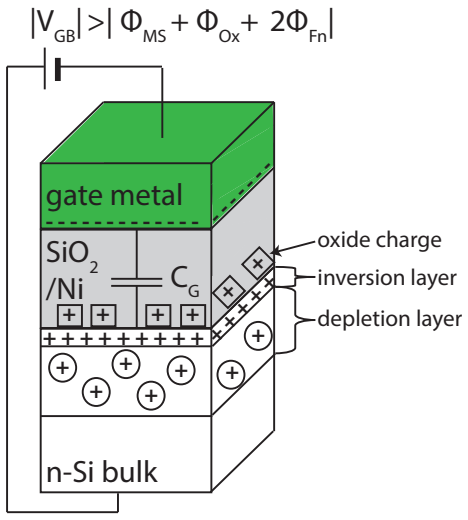
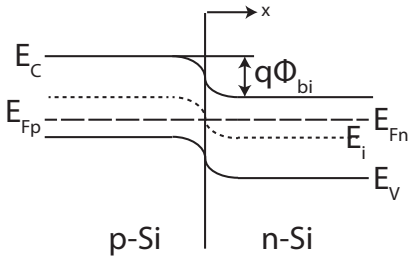


Figure 2.2.5.: The gate MOS structure as capacitor in strong inversion. The inversion layer of holes below the gate oxide and the depletion layer consisting of positive charged donor atoms are distinguished.

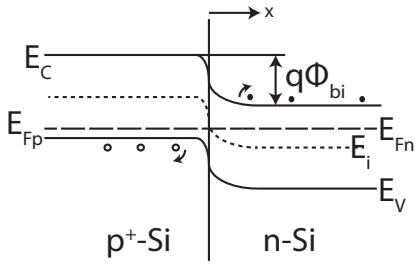
In order to build a sufficient electrical connection between source and drain, the negative gate voltage must ensure strong inversion with an upward bending of the semiconductor bands of at least $|\Phi| > |2\Phi_{\text{Fn}}|$. The gate MOS structure in strong inversion is depicted in figure 2.2.5. Due to the potential drop between gate and bulk V_{GB}, holes build the inversion layer charge per unit area $Q'_{\text{I}}(y)$ below the gate oxide and in addition ionized donor atoms in the bulk form a depletion layer.

Note, that the inspection of the MOS structure has been done using the so-called charge sheet model described i.a. in [28]. Therefore, it is considered that the electrons accumulated on the gate repel the odd valence electrons of the donor atoms in the bulk material up to a certain depth. The thus formed depletion layer is assumed to stay constant even when the gate voltage V_G is made more negative and the inversion layer is formed.

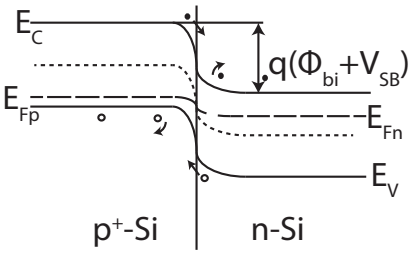
PN junctions of source and drain



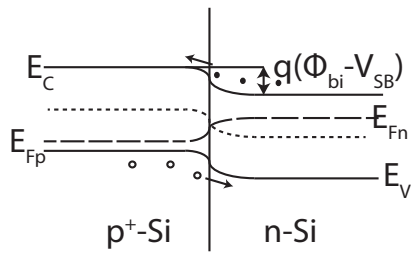
(a) Without external bias. The band bending regions in x direction are similar on the n and p side of the junction. The built-in potential Φ_{bi} is a barrier for majority charge carrier on both sides of the junction.



(b) When the dopant concentration at the p side is increased, the band bending regions change as well as the built-in potential Φ_{bi}.



(c) Reverse bias. The barrier for majority charge carrier is increased but minority carrier cross the junction.



(d) Forward bias. Majority charge carriers can cross the junction.

Figure 2.2.6.: Band structure of the pn junction from source to bulk. Dots on the conduction band E_C symbolize electrons and the circles below the valence band E_V holes. The possible moving directions of the charge is given by the arrows.

The band structure of the gate MOS of the transistor is influenced by the pn junctions of source and drain. To understand why, the energy band structure of a pn junction for four different states is shown in figure 2.2.6. The junction is considered to be abrupt.

1. A pn junction in thermal equilibrium is shown in figure 2.2.6a: If silicon doped with acceptor ions (p-Si) N_A is brought in contact with silicon doped in the

same order of magnitude with donor ions (n-Si) N_D, the Fermi energy levels E_{Fp} and E_{Fn} will be at the same level. Hence, the conduction E_C, intrinsic E_i and valence band E_V bend at a similar amount on both sides of the junction. The resulting potential step is referred to as built-in potential Φ_{bi}. Due to the doping, holes are the majority charge carriers in the p-Si and electrons respectively in the n-Si. Φ_{bi} is a barrier for these majority charge carriers. Thus, a depletion region on both sides of the junction is formed.

2. If the dopant concentration at the p side is increased several magnitudes compared to the n side, as displayed in figure 2.2.6b, the band bending regions will change as well as the built-in potential Φ_{bi}. The depletion depth on the n side will be deeper because of its lower doping concentration $N_A >> N_D$.

3. Applying a negative voltage between source and bulk V_{SB} to the p+ side increases the barrier and the depletion region (see figure 2.2.6b). This case is called reverse bias.

4. If the voltage at p+ is positive compared to the n side, the depletion region disappears and the majority charge carriers can cross the junction (see figure 2.2.6c). This is the so-called forward bias condition.

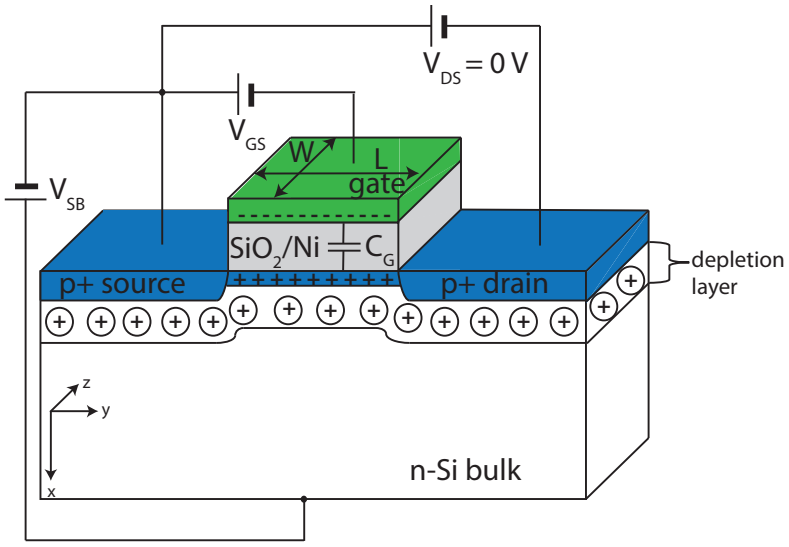


Figure 2.2.7.: PMOS with the MOS structure in strong inversion and no potential difference between source (S) and drain (D). The thickness of the inversion layer is constant and the depletion layers of MOS and pn junctions are connected.

When the gate MOS terminal is combined with the pn junction terminals of source and drain, as shown in figure 2.2.7, the junctions influence the inversion and depletion layer below the gate. When a potential difference is applied between source and drain, the thickness of the inversion layer, also referred to as channel thickness d_C, and the thickness of the depletion layer become a function of the coordinate y, as depicted in figure 2.2.8. At the drain terminal, the reverse bias condition is given and thus the depletion layer is broader than near the source. The inversion layer near the drain

is weakened with more negative voltage by the depletion layer charge $Q'_{\mathrm{D}}(y)$. Near the forward biased source pn junction the inversion layer is increased.

PMOS transistor current

Using the concepts from the last two sections, the transistor current characteristics can be derived. For a more detailed discussion see [29, 28, 33, 27]. For simplicity the following assumptions are made:

- the PMOS transistor geometry is linear with $A_{\mathrm{G}} = W \cdot L$.
- the bulk doping N_{D} is considered constant as well as the hole mobility μ_{p}.
- strong inversion starts at a band bending of two times the Fermi potential Φ_{F} below the gate.
- the contribution of interface traps between oxide and silicon to the threshold voltage V_{Th} is neglected.
- pn junctions are considered to be abrupt.
- the gate oxide is assumed to be a perfect isolator.

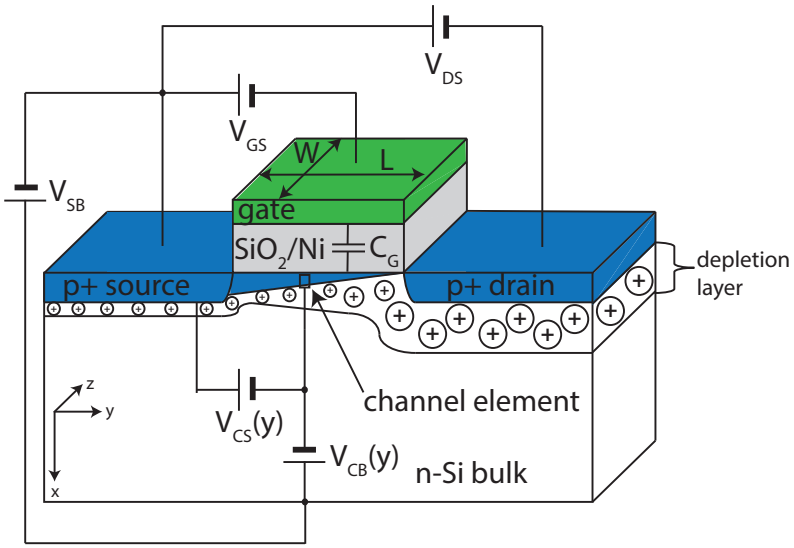


Figure 2.2.8.: PMOS with the MOS structure in strong inversion and the reverse bias condition at the drain. The thickness of the inversion layer, also referred to as channel thickness d_{C}, decreases from source to drain.

In general, the current I is defined as charge that moves through a channel cross section A_{C} per unit time. As mentioned in section 2.2.2 before, the charge carriers contributing to the current in a PMOS are holes. They move along the electrical connection path between source and drain also referred to as channel or inversion layer. For the current can be written

$$I = \rho \cdot A_{\mathrm{C}} \cdot v_{\mathrm{P}} \tag{2.2.5}$$

with the charge density per volume ρ, the channel cross section area A_C and the hole velocity v_P. The charge velocity results from the drift field between a channel element and the source V_{CS} multiplied with the charge mobility μ_P. Hence, we can rewrite v_P as

$$v_P = \mu_P \frac{\partial V_{CS}(y)}{\partial y} \tag{2.2.6}$$

In addition, the cross section area of the channel A_C can be substituted by the product of channel width W and channel thickness $d_C(y)$ at a certain position in y direction. Hence, the current becomes

$$I = \rho \cdot d_C(y) \cdot W \cdot \mu_P \frac{\partial V_{CS}(y)}{\partial y} \tag{2.2.7}$$

$\rho \cdot d_C(y)$ can be replaced by the channel charge per unit area $Q'_C(y)$. $Q'_C(y)$ are the holes in the inversion layer below the MOS gate that contribute to the current. Thus we can say $Q'_C(y) = Q'_I(y)$. When the MOS structure is considered as capacitor, as described above in equation 2.2.4 and figure 2.2.4, the charge accumulated at the metal-silicon oxide interface $Q'_G(y)$ is equal to the sum of the charge in the inversion layer $Q'_C(y)$ and the charge in the depletion layer of the junctions $Q'_D(y)$

$$Q'_C(y) = Q'_G(y) - Q'_D(y) \tag{2.2.8}$$

The charge carrier per unit area on the gate $Q'_G(y)$ result from the gate capacitance C_G and the applied gate voltage V_{GS} with respect to the source potential. As discussed for figure 2.2.4c, V_{GS} must overcome the natural band bending due to the contact potential Φ_{MS} and the oxide charge potential Φ_{Ox} as well as ensure strong inversion starting at $2\Phi_F$. In addition, the influence of the gate bias V_{GS} is weakened through the external drain voltage V_{DS}. This influence is dependent on the y position in the channel. Consequently, the potential drop between a channel element and the source V_{CS} is introduced. Thus we obtain

$$Q'_G(y) = -C'_G(V_{GS} - \Phi_{MS} - \Phi_{Ox} - 2\Phi_F - V_{CS}(y)) \tag{2.2.9}$$

The depletion layer charge can be described by

$$Q'_D(y) = \sqrt{2\epsilon_{Si}\epsilon_0 q N_D (2\Phi_F - V_{CB}(y))} \tag{2.2.10}$$

derived from the Poisson equation for the pn junction, which is given later in equation 2.2.22. Here, V_{CB} is the potential drop between the channel and the bulk. It can also be expressed by the sum of the potential between source and bulk V_{SB} and the potential between channel and source V_{CS}. When V_{CS} is considered small compared to V_{SB}, thus equation 2.2.10 becomes

$$Q'_D = \sqrt{2\epsilon_{Si}\epsilon_0 q N_D (2\Phi_F - V_{SB})} \tag{2.2.11}$$

Inserting equation 2.2.8 in 2.2.7 gives

$$I = (Q'_G(y) - Q'_D(y)) \cdot W \cdot \mu_P \frac{\partial V_{CS}(y)}{\partial y} \tag{2.2.12}$$

or written as integral

$$\int I \cdot \partial y = \int (Q'_{\mathrm{G}} - Q'_{\mathrm{D}}) \cdot W \cdot \mu_{\mathrm{P}} \cdot \partial V_{\mathrm{CS}} \tag{2.2.13}$$

From the linear PMOS structure in figure 2.2.8, it is known that the channel has the length L in the y direction. The potential drop between a channel element and the source V_{CS} is zero at a distance $y = 0$ from the source. At $y = L$ the element sees the full potential drop between source and drain V_{DS}. The integral of equation 2.2.13 written with the boundaries gives

$$\int_0^L I \cdot \partial y = \int_0^{V_{\mathrm{DS}}} (Q'_{\mathrm{G}} - Q'_{\mathrm{D}}) \cdot W \cdot \mu_{\mathrm{P}} \cdot \partial V_{\mathrm{CS}} \tag{2.2.14}$$

Integrating this with equations 2.2.9 and 2.2.11 inserted, the transistor current is obtained to be

$$I = -\frac{W}{L} \mu_{\mathrm{P}} C'_{\mathrm{G}} V_{\mathrm{DS}} \left(V_{\mathrm{GS}} - \Phi_{\mathrm{MS}} - \Phi_{\mathrm{Ox}} - 2\Phi_{\mathrm{F}} - \frac{V_{\mathrm{DS}}}{2} + \frac{\sqrt{2\epsilon_{\mathrm{Si}}\epsilon_0 q N_{\mathrm{D}} (2\Phi_{\mathrm{F}} - V_{\mathrm{SB}})}}{C'_{\mathrm{G}}} \right) \tag{2.2.15}$$

Summarizing values expressing the onset of the transistor current as threshold voltage

$$V_{\mathrm{Th}} = \Phi_{\mathrm{MS}} + \Phi_{\mathrm{Ox}} + 2\Phi_{\mathrm{F}} - \frac{\sqrt{2\epsilon_{\mathrm{Si}}\epsilon_0 q N_{\mathrm{D}} (2\Phi_{\mathrm{F}} - V_{\mathrm{SB}})}}{C'_{\mathrm{G}}} \tag{2.2.16}$$

leads to the well known expression for the current of a PMOS transistor

$$I_{\mathrm{PMOS}} = -\frac{W}{L} \cdot \mu_{\mathrm{P}} \cdot C'_{\mathrm{G}} \left(V_{\mathrm{GS}} - V_{\mathrm{Th}} - \frac{V_{\mathrm{DS}}}{2} \right) \cdot V_{\mathrm{DS}} \tag{2.2.17}$$

Equation 2.2.17 is only valid when the channel has the length L in the so-called linear region. When V_{DS} is increased above the saturation voltage $V_{\mathrm{DS,sat}} = V_{\mathrm{GS}} - V_{\mathrm{Th}}$, the length of the inversion layer gets shorter than L. This effect is also referred to as pinch off. Inserting $V_{\mathrm{DS,sat}}$ in equation 2.2.17 gives the PMOS current for the saturation region

$$I_{\mathrm{PMOS}} = -\frac{W}{2L} \cdot \mu_{\mathrm{P}} \cdot C'_{\mathrm{G}} \left(V_{\mathrm{GS}} - V_{\mathrm{Th}} \right)^2 \cdot (1 - \lambda V_{\mathrm{DS}}) \tag{2.2.18}$$

I_{PMOS} increases further in the saturation region due to the reduction of the effective channel length, which is represented by the channel length modulation parameter λ. λ can also be expressed by $\frac{1}{V_{\mathrm{Early}}}$. The Early voltage V_{Early} is known from space charge widening of junction transistors [34].

The transistor characteristics constant is introduced as

$$\beta = \frac{W}{L} \cdot \mu_{\mathrm{P}} \cdot C'_{\mathrm{G}} \tag{2.2.19}$$

In order to deduce the conductance parameter of the PMOS transistor, I_{PMOS} in the saturation region is differentiated with respect to V_{GS} or V_{DS}. The gate transconductance is given by

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{PMOS}}}{\partial V_{\mathrm{GS}}} = -\beta (1 - \lambda \cdot V_{\mathrm{DS}}) \left(V_{\mathrm{GS}} - V_{\mathrm{Th}} \right) \tag{2.2.20}$$

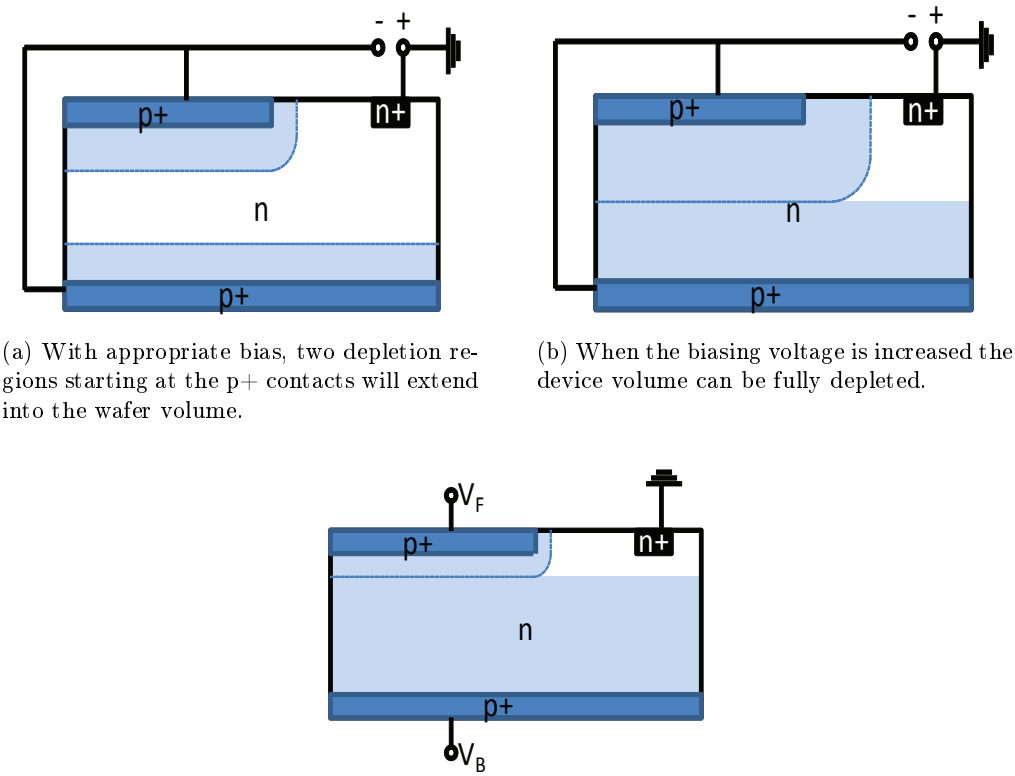
and the output conductance by

$$g_0 = \frac{\partial I_{\mathrm{PMOS}}}{\partial V_{\mathrm{DS}}} = \frac{\beta \cdot \lambda}{2} (V_{\mathrm{GS}} - V_{\mathrm{Th}})^2 \tag{2.2.21}$$

2.2.3. Detection principle

As mentioned in section 2.2.1, the PMOS of the DEPFET is operated on a fully depleted bulk in order to detect ionizing radiation.

Sidewards depletion



(a) With appropriate bias, two depletion regions starting at the p+ contacts will extend into the wafer volume.

(b) When the biasing voltage is increased the device volume can be fully depleted.

(c) If $V_{\mathrm{B}} << V_{\mathrm{F}} < 0$ V, the potential minimum will shift from the device center towards the front side.

Figure 2.2.9.: Principle of sidewards depletion.

The DEPFET operating principle is based on sidewards depletion, which was proposed by Gatti and Rehak in 1984 [35]. In figure 2.2.9 a n-substrate wafer with p+ implantation at front and back side as well as an additional n+ contact is shown. The two pn junctions are reverse biased. Their depletion regions will extend in the substrate as displayed in figure 2.2.9a. When the bias voltage is increased, the regions extend further into the wafer until the volume is fully depleted, see figure 2.2.9b. The potential minimum for electrons is then located at the center of the wafer. The position of the potential minimum can be shifted by applying different voltages at

front and back side, for example by choosing a more negative voltage for the back side V_{B} than the front V_{F} as presented in figure 2.2.9c. The position of the minimum can be obtained by using Poisson equation

$$\frac{\partial^2 \Phi}{\partial x^2} = -\frac{\partial \mathcal{E}}{\partial x} = -\frac{\rho(x)}{\epsilon_{\mathrm{Si}}\epsilon_0} \tag{2.2.22}$$

The charge density per volume of the n-Si bulk is given as

$$\rho(x) = q \cdot N_{\mathrm{D}} \tag{2.2.23}$$

assuming a constant doping concentration N_{D}. q is the magnitude of electronic charge with $1.602 \cdot 10^{-19}$ As. The electric field $\mathcal{E}$ is derived by integrating equation 2.2.23 with respect to x from 0 to the wafer thickness d. The force on electrons is zero where the depletion regions are in contact or overlap. The depth of the depletion regions is proportional to the applied voltages V_{F} and V_{B}. Thus the integration constant is obtained using the boundary condition $\mathcal{E}(x = \frac{d}{2}) = \frac{V_{\mathrm{B}} - V_{\mathrm{F}}}{d}$. This leads to

$$\mathcal{E}(x) = \frac{q \cdot N_{\mathrm{D}} \cdot d}{2\epsilon_{\mathrm{Si}}\epsilon_0} + \frac{q \cdot N_{\mathrm{D}} \cdot d \cdot x}{\epsilon_{\mathrm{Si}}\epsilon_0} - \frac{V_{\mathrm{B}} - V_{\mathrm{F}}}{d} \tag{2.2.24}$$

Integrating equation 2.2.24 with respect to x results in the potential distribution. The potential at the front and back side equals the external bias V_{F} and respectively V_{B}. The boundary condition $\Phi(x = 0) = V_{\mathrm{F}}$ is used to determine the integration constant. Hence, the potential is described by

$$\Phi(x) = \frac{q \cdot N_{\mathrm{D}} \cdot d \cdot x}{2\epsilon_{\mathrm{Si}}\epsilon_0} - \frac{q \cdot N_{\mathrm{D}} \cdot d \cdot x^2}{2\epsilon_{\mathrm{Si}}\epsilon_0} + \frac{(V_{\mathrm{B}} - V_{\mathrm{F}}) \cdot x}{d} + V_{\mathrm{F}} \tag{2.2.25}$$

The potential minimum for electrons is located where $\mathcal{E}(x) = 0$, that means at

$$x_{\mathrm{Min}} = \frac{d}{2} + \frac{\epsilon_{\mathrm{Si}}\epsilon_0 (V_{\mathrm{B}} - V_{\mathrm{F}})}{q \cdot N_{\mathrm{D}} \cdot d} \tag{2.2.26}$$

The potential distribution $\Phi(y)$ for several V_{F} and V_{B} combinations is shown in figure 2.2.10. It shows that the potential minimum for electrons is shifted towards the front for more negative backside voltages V_{B}. When electron-hole-pairs are generated in the depleted wafer volume, the electrons are collected at the position of the most positive potential, which is referred to as potential minimum. The holes are driven to the backside and drained there.

In case of the DEPFET, the source contact acts as front side contact and the clear as the n+ contact necessary for the sidewards depletion. The lateral position of the potential minimum x_{Min} is influenced by an additional deep n-doping below the gate at the front side of the wafer, shown in figure 2.2.11. In figure 2.2.10 the dashed line emphasizes the change in the potential distribution for the added doping near the front side of the wafer: The potential minimum is increased. Due to the n-doping and the sidewards depletion the minimum persists independent of the on or off state of the DEPFETs PMOS transistor as long as V_{F} and V_{B} stay at the same potential.

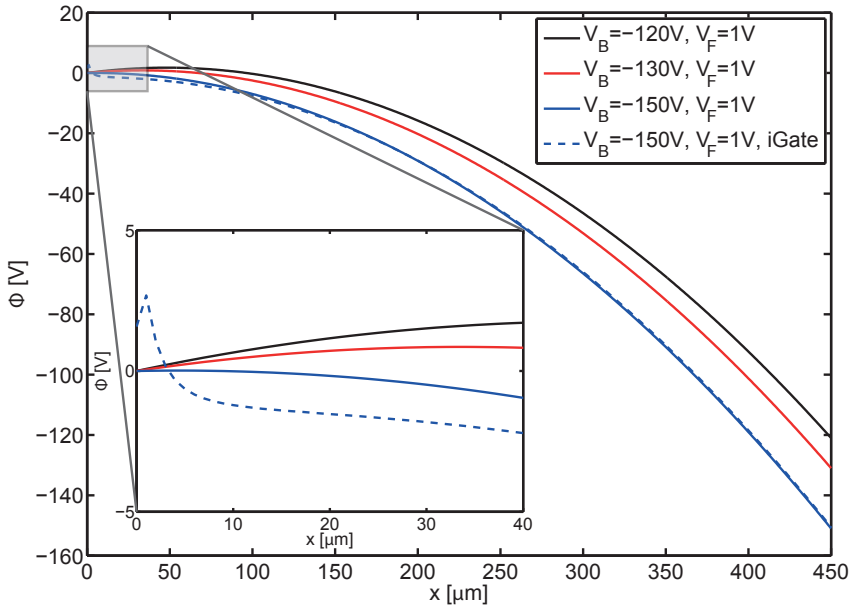


Figure 2.2.10.: Potential distribution from front side to back side for several V_F and V_B combinations. The wafer thickness is 450 µm. The inset shows a closeup of the potential distribution from the front side to a depth of 40 µm. The dashed line emphasizes the influence of an additional deep n-doping on the potential distribution, which is taken from simulations described in section 2.4.

Internal amplification

A fraction f[1] of the electrons collected below the transistor channel Q_iG, as depicted in figure 2.2.11, induces additional holes in the channel and thus modulates its conductivity. In other words, Q_iG controls the transistor current in a way similar to the external gate and therefore the potential minimum is referred to as internal gate. When holes are induced by the internal gate, the channel charge from equation 2.2.8 changes to

$$Q'_\mathrm{C}(y) = Q'_\mathrm{G}(y) - Q'_\mathrm{D}(y) + f \cdot Q'_\mathrm{iG} \tag{2.2.27}$$

It is assumed that the minimum is distributed equally underneath the transistor channel, which means it has the same area as the gate, hence $Q'_\mathrm{G}(y)$ from equation 2.2.9 can be written as

$$Q'_\mathrm{G}(y) = -C'_\mathrm{G}\left(V_\mathrm{GS} - \Phi_\mathrm{MS} - \Phi_\mathrm{Ox} - 2\Phi_\mathrm{F} - V_\mathrm{CS}(y) + \frac{f \cdot Q_\mathrm{iG}}{C_\mathrm{G}}\right) \tag{2.2.28}$$

Integrating with the same boundaries as used for equation 2.2.14 gives for the transistor current in the linear region

$$I_\mathrm{PMOS} = -\beta\left(\frac{f \cdot Q_\mathrm{iG}}{C_\mathrm{G}} + V_\mathrm{GS} - V_\mathrm{Th} - \frac{V_\mathrm{DS}}{2}\right) \cdot V_\mathrm{DS} \tag{2.2.29}$$

[1] A small amount of Q_iG does also induce charge in source and drain.

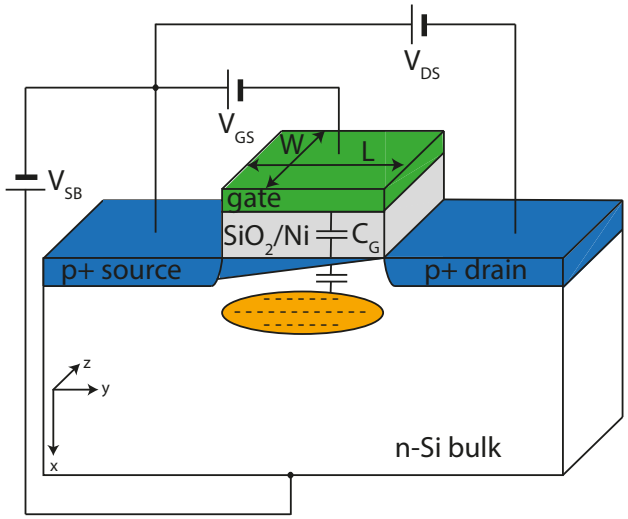


Figure 2.2.11.: Capacitive coupling of the internal gate (iG) into the PMOS transistor channel. The deep n-doping, which defines the position of the internal gate (iG), is marked orange. The internal gate is shown as filled with collected signal electrons here.

For the saturation region inserting $V_{\mathrm{DS,sat}} = V_{\mathrm{GS}} - V_{\mathrm{Th}} + \frac{f \cdot Q_{\mathrm{iG}}}{C_{\mathrm{G}}}$ in 2.2.29 leads to

$$I_{\mathrm{PMOS}} = -\frac{\beta}{2}\left(\frac{f \cdot Q_{\mathrm{iG}}}{C_{\mathrm{G}}} + V_{\mathrm{GS}} - V_{\mathrm{Th}}\right)^2 \cdot (1 - \lambda V_{\mathrm{DS}}) \tag{2.2.30}$$

As will be shown in section 4, the PMOS transistor of the DEPFET is usually operated in its saturation region because voltage changes for V_{GS} or V_{DS} do not lead to enormous shifts of I_{PMOS} as they would in the linear region. The conductance parameter in that region can be obtained by differentiating I_{PMOS} with respect to V_{GS} or V_{DS} as done before in equations 2.2.20 and 2.2.21. The gate transconductance is given by

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{PMOS}}}{\partial V_{\mathrm{GS}}} = -\beta \cdot (1 - \lambda \cdot V_{\mathrm{DS}}) \cdot \left(\frac{f \cdot Q_{\mathrm{iG}}}{C_{\mathrm{G}}} + V_{\mathrm{GS}} - V_{\mathrm{Th}}\right) \tag{2.2.31}$$

and the output conductance by

$$g_0 = \frac{\partial I_{\mathrm{PMOS}}}{\partial V_{\mathrm{DS}}} = \frac{\beta \cdot \lambda}{2}\left(\frac{f \cdot Q_{\mathrm{iG}}}{C_{\mathrm{G}}} + V_{\mathrm{GS}} - V_{\mathrm{Th}}\right)^2 \tag{2.2.32}$$

The conductance parameter for the current modulation induced by electrons collected in the internal gate is called charge transconductance g_{q} and it is defined as

$$g_{\mathrm{q}} = \frac{\partial I_{\mathrm{PMOS}}}{\partial Q_{\mathrm{iG}}} = -\frac{\beta \cdot f \cdot (1 - \lambda \cdot V_{\mathrm{DS}})}{C_{\mathrm{G}}} \cdot \left(\frac{f \cdot Q_{\mathrm{iG}}}{C_{\mathrm{G}}} + V_{\mathrm{GS}} - V_{\mathrm{Th}}\right) \tag{2.2.33}$$

Depending on the DEPFET design and bias conditions, charge transconductance g_{q} values of $200\,\frac{\mathrm{pA}}{e-}$ [36] to $1\,\frac{\mathrm{nA}}{e-}$ [37] have been measured so far. For detectors, the signal to noise ratio and thus the amplification of the signal is important. Combining g_{q} of

equation 2.2.33 and g_m of 2.2.31 respectively results in the internal amplification of the DEPFET

$$g_\mathrm{d} = \frac{g_\mathrm{q}}{g_\mathrm{m}} = \frac{f}{C_\mathrm{G}} \tag{2.2.34}$$

A typical internal amplification is $\approx 3.8\ \frac{\mu\mathrm{V}}{e^-}$ [13].

By remembering figure 2.2.1 it is apparent, that the DEPFET is a complex three-dimensional transistor structure. Hence, measured characteristics will deviate from the analytical ones derived here because of

- the potential drop between source and drain, which leads to a non-equal distribution of the internal gate underneath the MOS gate. Its center of gravity is near the source. This may lead to an overestimation of the I_PMOS steering by the internal gate as the current density has its maximum at the drain due to the circular shape of the MOS gate.
- due to the massive silicon oxide thickness $d_\mathrm{Ox} = 180$ nm, short channel effects like a threshold voltage V_Th shift may occur. This suggestion is supported by [38], in which is stated that transistors are considered to be short channel transistors, when the depletion depth of the pn junctions with applied voltages is in the same order of magnitude as the channel length L.

The analytical expressions derived in section 2.2.2 and 2.2.3 provide basic understanding of the main concepts of the DEPFET. For a more detailed three-dimensional analysis, simulations are needed in order to solve the Poisson equation numerically, see section 2.4.

Removal of signal charge

It is assumed that an X-ray photon of the energy E_Photon is completely absorbed in the fully depleted n-Si bulk of the DEPFET creating electron-hole pairs after equation 2.1.1. By means of the potential distribution, see again figure 2.2.10, the holes are driven to the back side and the electrons are collected in the internal gate. The signal electrons Q_iG induce additional holes in the channel of the PMOS and therefore increase the transconductance g_m of the transistor. Hence, I_PMOS increases for a fixed V_DS or V_DS decreases for a fixed I_PMOS. $\Delta\ I_\mathrm{PMOS}$ or $\Delta\ V_\mathrm{DS}$ respectively are proportional to the amount of signal charge Q_iG as proven by equation 2.2.29. In order to extract the signal information, the transistor current I_PMOS or the potential drop between source and drain V_DS is measured with filled and with empty internal gate. The difference of these two correlated measurements gives $\Delta\ I_\mathrm{PMOS}$ or $\Delta\ V_\mathrm{DS}$ and thereby E_Photon can be determined. This measurement method is called Correlated Double Sampling (CDS).

The NMOS transistor of the DEPFET, the so-called clear structure, is needed to remove Q_iG from the internal gate during the CDS readout of the DEPFET. Figure 2.2.12 shows a filled internal gate below the gate MOS structure and the adjoining clear structure. The internal gate is separated from the clear contact through the depletion region of the deep p-well when the clear gate MOS structure is biased negative. The clear potential V_C is kept more negative than the potential of the internal

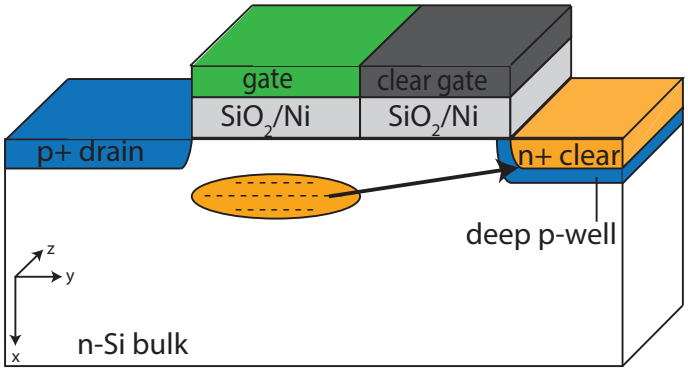


Figure 2.2.12.: Part of the DEPFETs PMOS structure with the adjoining clear NMOS. The internal gate (iG) below the gate (G) is filled with signal electrons. By applying a sufficient positive clear gate (CG) and clear (C) voltage the electrons overcome the depletion region of the p-well and are drained through the clear (C) contact.

gate to avoid charge loss during the charge integration. This state of clear and clear gate is referred to as off state. In order to remove Q_{iG} from the internal gate, the clear contact is set to a more positive potential as the internal gate to attract the signal electrons Q_{iG}. The clear gate barrier is opened by applying a sufficiently positive voltage. Now an electrical connection from internal gate to the clear contact is established and the electrons are removed through the clear contact. After the removal of the signal charge, the clear gate is set back to the off state followed by the clear contact. As can be seen later in section 2.2.5, the switching of clear gate and clear is done in this particular order because otherwise, when the clear gate is opened before the clear potential is in on state or closed after the clear is in off state, the clear potential is more negative than the internal gate and electrons would move from clear to internal gate for the switching time and contaminate the signal information.

2.2.4. DEPFET matrix

So far, only single pixels have been considered. To increase the detection area of the X-ray sensor and allow spectroscopic imaging, a matrix of several DEPFET pixels is needed. By looking at the DEPFET equivalent circuit depicted in figure 2.2.13 it becomes clear that a DEPFET matrix can be formed by arranging several single DEPFET pixels in a grid as done here for a 2×2 matrix. Various interconnection schemes are possible. For the most common interconnection structure the clear, clear gate and gate contacts of all pixels are connected in rows and the source contacts in columns. The drain is biased globally as grid. For this configuration the DEPFET pixels can be addressed row-wise in rolling shutter mode and read out individually in parallel at the source. In case a drain readout is targeted, the connection of source and drain as grid and in columns are realized in reverse.

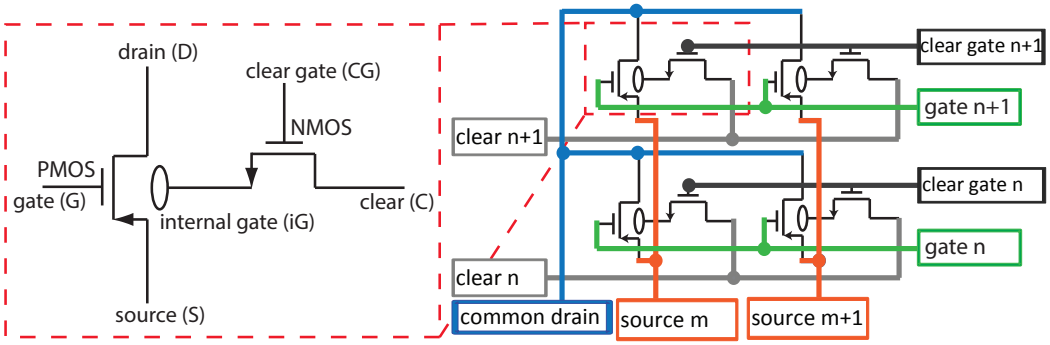


Figure 2.2.13.: A DEPFET matrix can be formed by arranging several single DEPFET pixels in an array and connecting their bias contacts in rows and columns. In this example, the drain is realized as common grid contact so that the DEPFET can be read out at the source.

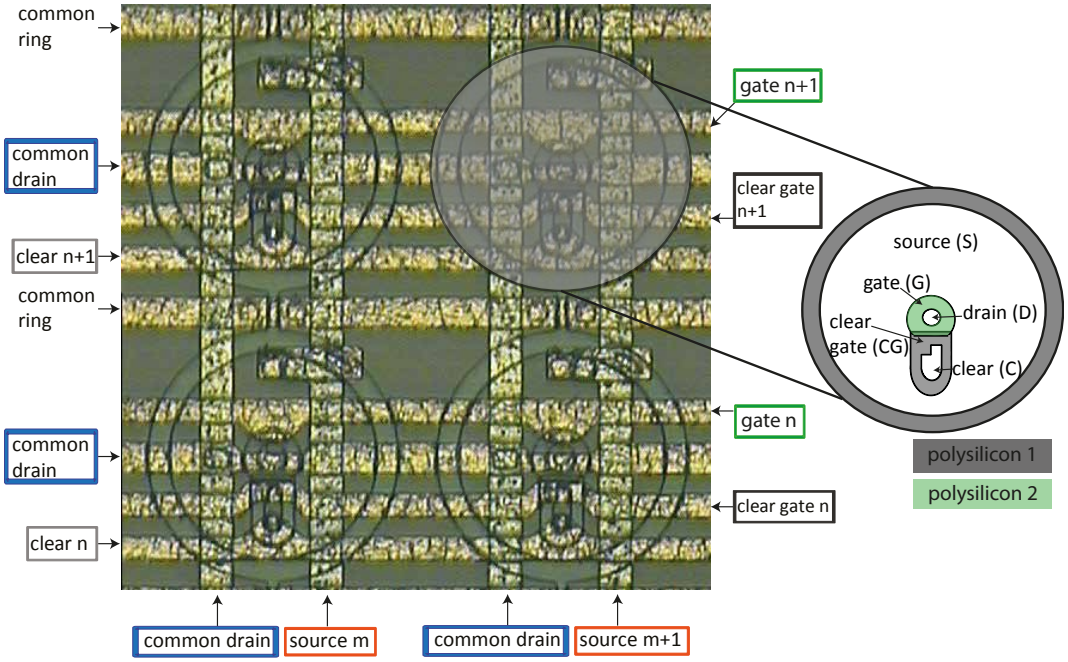


Figure 2.2.14.: The microscope image shows a 2 × 2 pixel part of a DEPFET matrix covering an area of 200 × 200 μm^2. The polysilicon structures of the DEPFET and the ring on top of the silicon bulk material can be seen as well as the aluminium wiring. The wiring connections are named like in the schematic in figure 2.2.13.

When DEPFETs are combined for a rolling shutter mode matrix, three global contacts are added:

1. Ring (R1): In order to provide spatial resolution, it is essential to separate the potential of neighboring DEPFET pixel. Therefore the ring is located in between the pixels and builds a grid over the matrix that is set to a negative voltage. A potential gradient for electrons towards the internal gate of the pixels is formed. This ring separates the pixels. The ring potential is separated from the source via a circular polysilicon spacer shown in figure 2.2.14.

2. Inner substrate (InS): When polysilicon structures like the circular potential separator are located on top of a silicon substrate, electron-hole pairs are generated at the interface. The resulting surface leakage current is drained with the global inner substrate contact, which can be biased as positive as the clear contact.

3. Outer substrate (OS): The outer substrate surrounds the grid of pixels to prevent the border pixels from leakage currents of the chip periphery produced e.g. by thermal generation at the bond pads of the chip.

A microscope image of a 2 × 2 pixel part of a DEPFET matrix is displayed in figure 2.2.14. In addition to the gate, drain, source, clear and clear gate shown in schematic 2.2.13, the wiring connection of the ring can be seen.

2.2.5. Readout mode

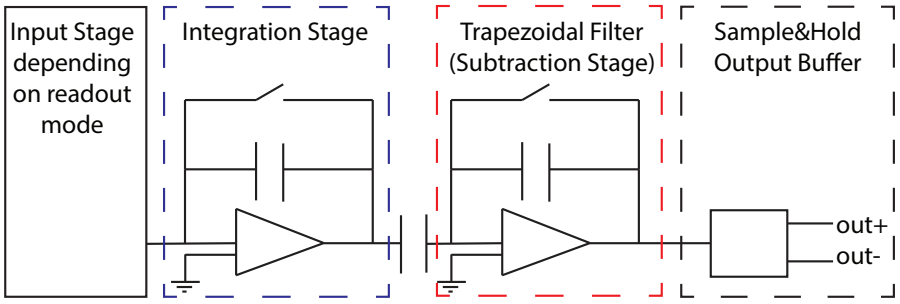
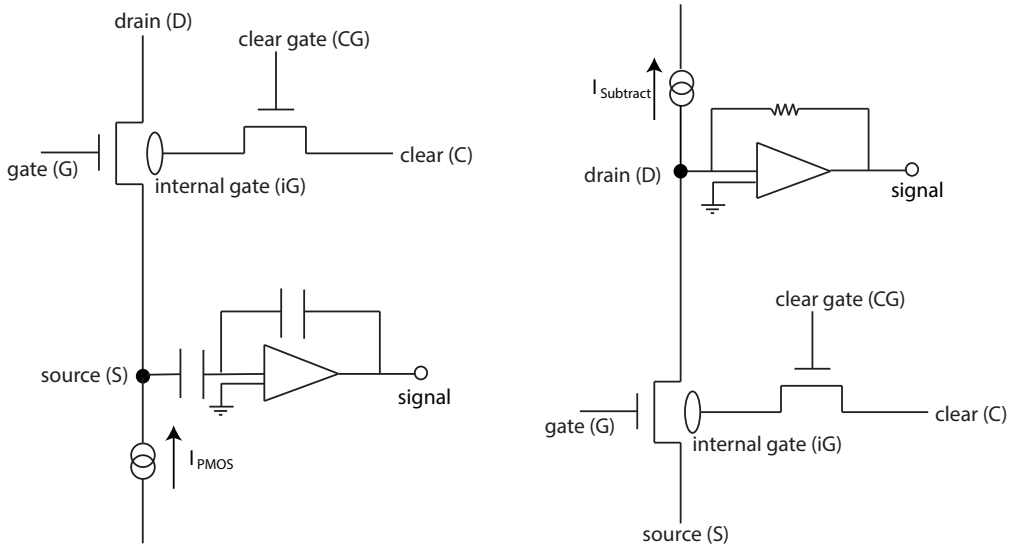


Figure 2.2.15.: Schematic of a typical readout chain included in an Application Specific Integrated Circuit (ASIC) for time variant filtering. Depending on the used readout mode, the input stage is implemented as shown later in figure 2.2.16. The integration, subtraction and output stage stay the same.

DEPFET matrices are usually read out using a special Application Specific Integrated Circuit (ASIC) because of their lower power and higher integration density in comparison to readout boards. Figure 2.2.15 depicts the schematic of a typical readout chain included in such an ASIC. The design of the input stage depends on the readout mode, as shown in figure 2.2.16, but all other stages can be the same. The signal information can be extracted at the source or the drain node of the DEPFET. Accordingly, the source is connected column-wise and the drain as grid or the other way round as mentioned in section 2.2.4. The modulated transconductance g_m can be measured either by fixing the source-drain voltage V_DS leading to ΔI_PMOS or by fixing I_PMOS leading to ΔV_DS. The measurement of ΔI_PMOS is usually done at the drain node thus it is called drain readout and the extraction of ΔV_DS is done at the source node and referred to as source follower readout, see table 2.2.1. It is also possible to include both input stages in one chip as done for the VErsatile Readout based on Integrated Trapezoidal Analog Shapers (VERITAS2.0) ASIC, which is currently under development [39].

A DEPFET is read out using CDS with the two samples usually taken as integrations of the signal levels before and after clear over a shaping time τ. The second sample



(a) The transistor current is fixed and the modulation of the source node potential is detected in the so-called source follower (SF) readout mode.

(b) The drain node potential is fixed and the transistor current modulation is detected in the so-called drain readout (DR) mode.

Figure 2.2.16.: Simplified schematic drawing of the input stages for the different DEPFET readout modes.

is subtracted from the first by a trapezoidal filter in the subtraction stage. The last stage is the sample and hold and a differential output buffer. The applied CDS readout sequence for both modes is presented in figure 2.2.17. It is assumed that an X-ray photon was absorbed and the signal electrons were collected in the internal gate. Either the current I_{PMOS} or the voltage V_{DS} is fixed by a current source in the readout ASIC for the source follower readout mode or a voltage source respectively for the drain readout. When the DEPFET is read, the PMOS transistor must be run in its saturation region by applying a sufficiently negative V_{GS}. Now the signal charge in the internal gate modulates the transconductance g_{m} of the transistor channel leading to a decreased V_{DS} or increased I_{PMOS}. The readout ASIC integrates the combined signal and baseline information during t_{Read1}. Then the clear and clear gate are activated to remove all electrons stored in the internal gate as described in section 2.2.3. Afterwards they are deactivated and the integration during t_{Read2} of the baseline starts. At last the two correlated measurements are subtracted giving $\Delta\ V_{\mathrm{DS}}$ or $\Delta\ I_{\mathrm{PMOS}}$.

For the spectroscopic DEPFET detector test described in chapter 4 the Active current Switching Technique ReadOut In x-ray spectroscopy with DEPFET (ASTEROID) has been used. Hence, the focus in the following lies on the source follower readout.

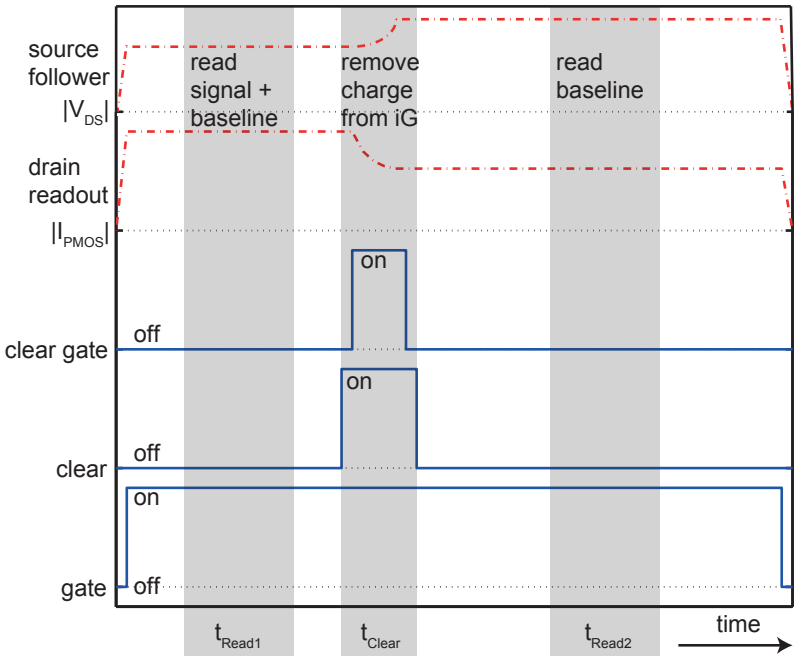


Figure 2.2.17.: When the DEPFET is read with CDS, the gate (G) must remain active all the time. The readout ASIC integrates the signal and baseline information during t_{Read1}. Then the clear (C) and clear gate (CG) are activated to remove all electrons stored in the internal gate (iG). Afterwards they are deactivated. Then the integration during t_{Read2} of the baseline starts and is subtracted from the first integration.

	source follower (SF) readout	**drain readout (DR)**
readout node	source (S) (see figure 2.2.16a)	drain (D) (see figure 2.2.16b)
fixed parameter	I_{PMOS}	V_{DS}
measured parameter	$\Delta\ V_{\mathrm{DS}}$	$\Delta\ I_{\mathrm{PMOS}}$
advantage	greater dynamic input range, better radiation damage tolerance	faster readout
disadvantage	slower readout due to capacitance coupling	must cope with production inhomogeneity of pixels
usable ASIC	ASTEROID [40, 41, 42]	VELA [43, 44]

Table 2.2.1.: Comparison of the source follower (SF) and drain readout (DR).

Readout noise using source follower mode with ASTEROID

The achievable readout noise of a DEPFET in source follower configuration in combination with the ASTEROID ASIC can be calculated by convoluting the noise power density of the DEPFET with the transfer function of the readout filter. The Equivalent Noise Charge (ENC) can be determined using [45]

$$ENC^2_{\mathrm{Filter}} = \frac{a}{\tau} C^2_{\mathrm{Det}} A_1 + 2\pi a_f C^2_{\mathrm{Det}} A_2 + b\tau A_3 \tag{2.2.35}$$

for a trapezoidal filter function with a shaping time τ, which equals t_{Read}.

The noise power densities of the DEPFET include

- a as amplitude of the thermal noise. It is also called white noise and it occurs due to the statistical movement of charge carrier.
- a_f as amplitude of the series $\frac{1}{f}$-noise. This noise is induced from crystal imperfections and traps in the transistor channel region.
- b represents the contribution of leakage current I_Leak with $b = 2 \cdot (-q) \cdot I_\mathrm{Leak}$ in the DEPFET and is also referred to as shot noise.

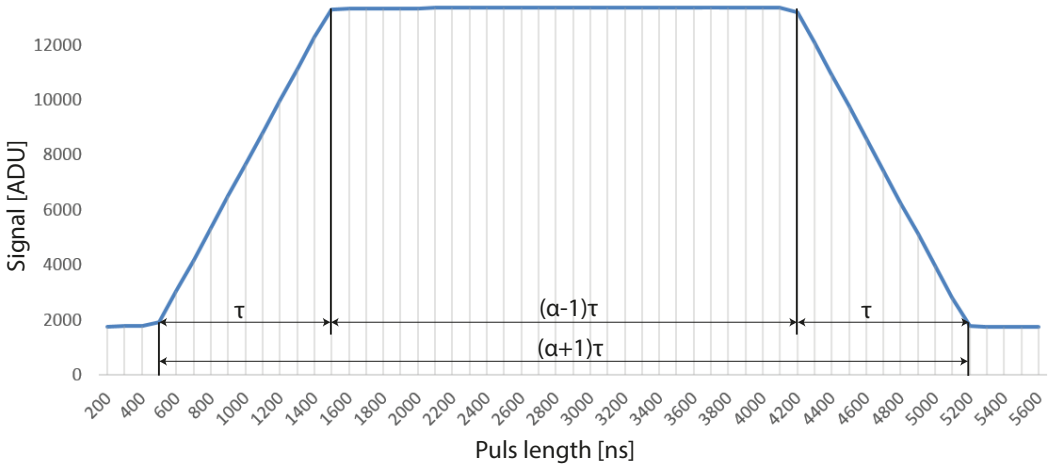


Figure 2.2.18.: Measured trapezoidal weighting function of the ASTEROID ASIC.

For a detailed description of the noise contributions see [46, 47]. The weighting parameters of the trapezoidal filter function are calculated according to [48]

$$A_1 = 2 \tag{2.2.36}$$

$$A_2 = \frac{1}{\pi}\left[(\alpha+1)^2 \cdot ln(\alpha+1) + (\alpha-1)^2 \cdot ln(\alpha-1) - 2\alpha^2 \cdot ln\alpha\right] = 1.78 \tag{2.2.37}$$

$$A_3 = \alpha - \frac{1}{3} = 3.32 \tag{2.2.38}$$

using the parameters α =3.65 and τ =1 µs extracted from the measured weighting function of the ASTEROID, as shown in figure 2.2.18. The DEPFET equivalent input capacitance C_Det as well as a and a_f are typically C_Det = 40 fF, $a = 1.53 \cdot 10^{-16}\ \frac{\mathrm{V}^2}{\mathrm{Hz}}$ and $a_\mathrm{f} = 4.5 \cdot 10^{-12}\ \mathrm{V}^2$ [49].

The ENC has a significant influence on the spectroscopic performance of the DEPFET and limits the FWHM. Thus, equation 2.1.4 changes to

$$FWHM = 2.355 \cdot E_{\text{e-h+}} \cdot \sqrt{ENC^2_\mathrm{Filter} + Fano^2} \tag{2.2.39}$$

The DEPFET collects signal charge until it is cleared. That means for matrix operation it collects as long as the other pixels are read resulting in a collection or also called integration time t_{Int} equal to the frame processing time t_{Frame} of the matrix minus one row time t_{Row}. During this time, the DEPFET also accumulates a small amount of leakage current I_{Leak} due to thermal charge generation in silicon at its operation temperature of approximately -55 °C. The leakage noise contribution is calculated using

$$N_{\mathrm{Leak}} = \sqrt{I_{\mathrm{Leak}} \cdot t_{\mathrm{int}}} \tag{2.2.40}$$

Adding this noise to equation 2.2.39 leads to an achievable FWHM of

$$FWHM = 2.355 \cdot E_{\text{e-h+}} \cdot \sqrt{ENC^2_{\mathrm{Filter}} + N^2_{\mathrm{Leak}} + Fano^2} \tag{2.2.41}$$

2.3. Design variants of the DEPFET

In order to improve the detector behavior with respect to the requirements of Athena, four different DEPFET designs are studied in this thesis. In this section a brief overview of the IS device design is given.

2.3.1. Overview of devices

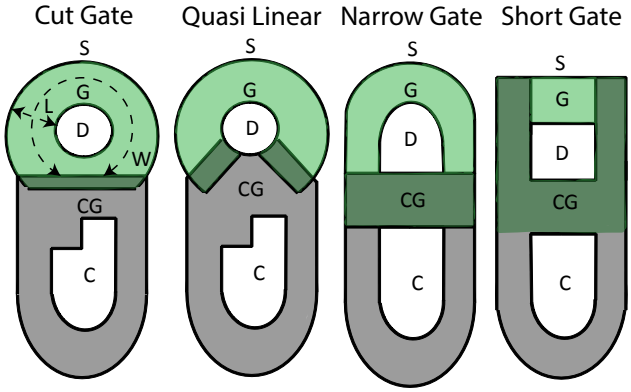


Figure 2.3.1.: Schematic drawing of the four DEPFET design variants. The cut gate design is the well known baseline. The gate (G) area is highlighted green and the clear gate (CG) area gray. The darker green shade marks the overlapping region of those two areas. The drain (D) is always in the center of the gate (G) and the source (S) is the surrounding contact.

Four DEPFET design variants, as shown in figure 2.3.1, have been studied. The DEPFET is embedded in the center of each pixel. The designs are close to circular structures because this allows a better usage of the pixel area than for linear structures at a squared pixel size of 100 µm × 100 µm. In all variants the p+ contact, which is foreseen for the negative bias (drain), is located in the center of the gate. The positively biased p+ source is the outer contact surrounding the gate. The drain centered pixel design is preferred since discovering charge losses due to a parasitic

potential minimum near the clear contact for source centered devices as discussed in [36]. The differences of the variants are the size of n+ clear and p+ drain contacts, clear gate dimension and shape as well as overlapping area of gate and clear gate.

	Cut Gate	Quasi Linear	Narrow Gate	Short Gate
$\frac{W}{L}$	7.33	6.19	8.97	2.41
A_G [μm^2]	181	166	70	20

Table 2.3.1.: Relation between gate width W and length L for the different DEPFET designs.

A significant parameter to further describe the differences between the DEPFET designs is the relation of the gate width W to length L presented in table 2.3.1. The cut gate design is used as well known default [20]. The quasi linear variant is the most similar to cut gate. The difference lies in a cut in the gate that allows the clear gate to touch the drain region without increasing the overlap between gate and clear gate. A minimum overlap is chosen due to uncertainties about the potential distribution and the existence of potential barriers between clear and internal gate. A lower barrier accelerates the clear process and decreases the needed clear voltage, which will be discussed later in section 3.3. For narrow gate and short gate structures, the gate area A_G is minimized, resulting in a higher amplification of the collected signal charge. A higher gain is expected to increase the signal to noise ratio of spectroscopic measurements, as will be experimentally verified in section 4.5. The down-scaling of the DEPFET is limited by the given minimum technological feature size of 2 µm to 3 µm [50].

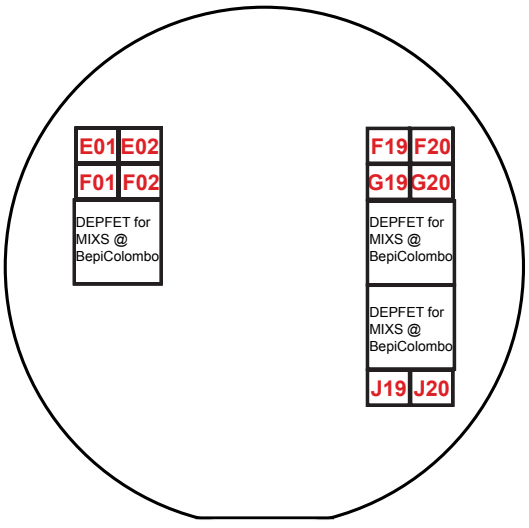


Figure 2.3.2.: Allocation of the IS chips as well as the MIXS devices on the wafer of the prototype production. The red character strings are the device names.

As mentioned in chapter 1, the IS prototypes are distributed over the wafer area to

study the property diversity and the homogeneity of the wafer production process. The layout of the wafer is shown in figure 2.3.2. The small numbered devices are the IS chips and the three larger ones are MIXS flight devices for the BepiColombo mission, which are similar to the IS prototypes. The MIXS devices are cut gate structures with three additional drift rings.

Chip	**Readout mode**		**DEPFET design**			
	DR	SF	CuG	QL	NG	SG
E01		X		X		
E02	X		X			
F01		X			X	
F02	X				X	
F19		X	X			
F20		X	X			
G19		X			X	
G20		X	X			
J19		X				X
J20	X		X			

Table 2.3.2.: IS devices per wafer: SF = Source Follower, DR = Drain Readout, QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate.

The IS prototypes consist of 64 × 64 DEPFET pixels. Each pixel covers an area of 100 × 100 μm^2 giving an active area of 0.41 cm^2. The total chip size including bond pads is 1.2 cm^2. The 10 IS structures per wafer vary in design and readout mode as listed in table 2.3.2. The only difference between source follower and drain readout chips is that either the sources of the DEPFETs are connected column-wise and the drain globally as grid as explained in section 2.2.4 or vice versa.

2.4. Simulation

For a deeper understanding of the analysis and discussion of the measurement data in chapters 3 and 4, DEPFET structures were simulated. The simulation software is briefly presented in the following sections.

2.4.1. Doping profile simulation using DIOS

The simulation process is explained on the example of the potential distribution in the DEPFETs PMOS. Thus, a cut section through drain, gate and source of a cut gate device, as presented in figure 2.4.1, is used.

At first the doping profile is simulated using the DIOS software from *SYNOPSYS* [51]. In DIOS the entire technology process for the front side of the wafer including layer deposition, ion implantation, diffusion, oxidation and etching is implemented. The wafer thickness was chosen to be 280 µm because it was found, that the simulation results for a 280 µm thick bulk is applicable to a 450 µm thick bulk in reality.

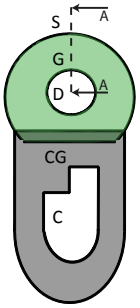


Figure 2.4.1.: Overview of the cut gate (CuG) design including the cut section A used for simulations of the DEPFETs PMOS transistor. The section is 20 µm long. It starts in the center of the drain (D) region and reaches 10 µm into the source (S) region.

However, fewer simulation grid points are needed while simplifying the calculations and speeding up the simulation process significantly. The front part of the resulting profile is shown in figure 2.4.2.

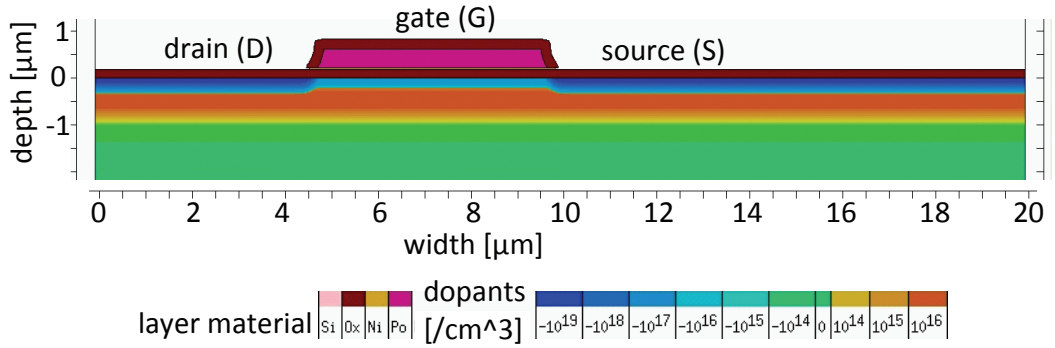


Figure 2.4.2.: Front part of the doping profile simulated with DIOS for the cut section through drain (D), gate (G) and source (S) shown in figure 2.4.1: Above the wafer surface the polysilicon gate with a nitride layer below and the silicon oxide layer is shown. Below the surface the p-doped drain and source regions can be seen as well as the increased n-doping below the transistor channel.

In figure 2.4.2 the polysilicon gate and gate oxide as well as the p-implanted drain and source regions with their dimensions can be seen. Furthermore, the increased n-doped region below the transistor channel is depicted. As shown in the next section, this region forms the potential minimum for electrons, the so-called internal gate. The resulting doping profile is used for further simulations.

2.4.2. DEPFET simulation using TeSCA

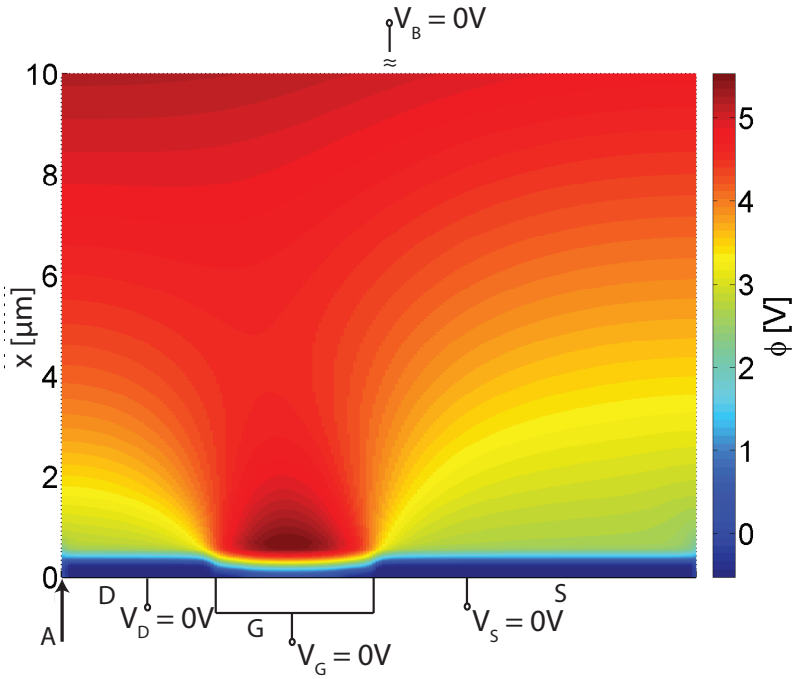
The next step is to define a grid for the two-dimensional finite element calculations with fine mesh at the front and back side of the wafer, due to the small doping gradients, and a rough one for the bulk using an automated grid generator provided by

the TeSCA software [52]. This grid then will be used by TeSCA for the simulation of the transfer characteristics of the DEPFET.

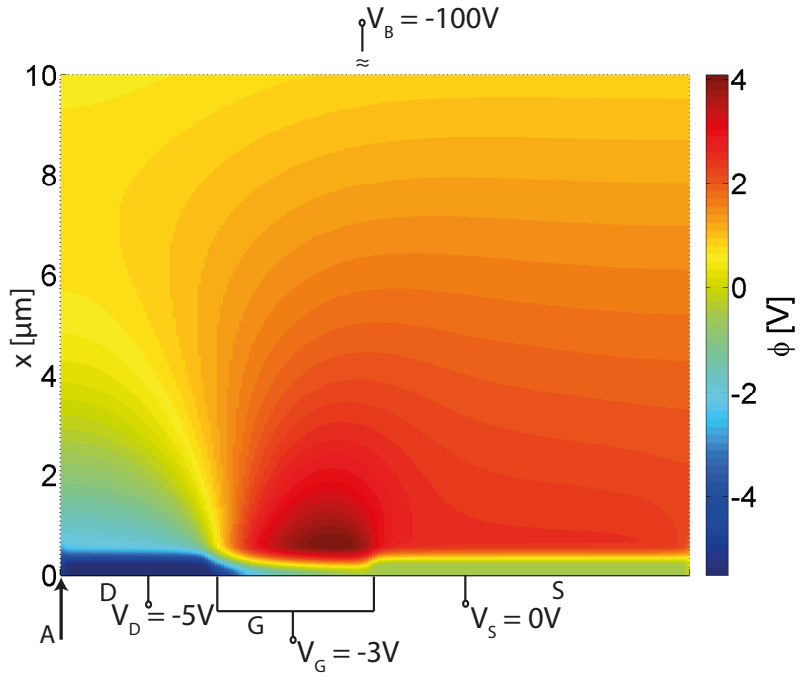
In order to approach the three dimensional structure of the DEPFET, a defined cut section is either rotated about the center of the drain or it is extruded. Both methods are of limited significance as they cannot model the influence of the clear structure. Even if the cut section includes parts of the clear structure, it is not possible to form the DEPFET out of a two dimensional cut because the DEPFET is neither a fully circular structure nor a linear one. This should be kept in mind while interpreting the simulation results. The simulations help to improve the understanding of the device but are not an image of the reality.

In case of the cut gate cut section defined in figure 2.4.1, the rotation about the center of the drain is chosen. The PMOS transistor bulk is depleted throughout the simulations. A simulation step is implemented, for which no external voltages are applied and only the Poisson equation (see equation 2.2.22) is solved until the equilibrium state is reached. A potential plot for the equilibrium state without external bias can be seen in figure 2.4.3a. For simulation steps with external bias in addition to the Poisson equation, the transport equation [52] is solved. An example bias scenario is depicted in figure 2.4.3b.

The internal gate is visible in both potential plots as potential minimum for electrons below the gate. Every electron produced in the bulk due to electron-hole pair generation will drift towards the internal gate as explained before in section 2.2.3. With external bias the center of gravity of the minimum is shifted towards the source contact as mentioned in section 2.2.3.



(a) Potential plot of the DEPFETs PMOS in equilibrium.



(b) Potential plot of the DEPFETs PMOS with external bias.

Figure 2.4.3.: Potential plot for a width of 20 µm and a depth of 10 µm of the simulated cut section. The drain (D) reaches from width 0 to 4.5 µm, the gate from 4.5 to 10.5 µm and the source region covers the rest. The internal gate (iG) is visible as potential minimum for electrons.

3. Electrical qualification measurements

The electrical qualification measurements analyze the PMOS and NMOS transistor of the DEPFET separately under quasi-static conditions. In the following sections the measurement setup for the electrical qualification is presented as well as measurement routines and results.

3.1. Scope of the electrical measurements

The purpose of the electrical qualification tests on die-level is fast yield and technology learning and, most important, device characterization. Using the measurement setup and routines described in section 3.2, within a few hours, the functionality of a device can be verified, technology problems like short-circuits found and the device homogeneity can be investigated. As the integration of a full detector with DEPFET matrix and ASICs is time consuming and expensive, the devices must be pre-qualified to avoid building a low-performance or defective detector system. With regard to the needed wafer-scale detectors for Athena, the device yield and homogeneity are evaluated in section 3.4 based on the electrical qualification data presented in section 3.3. In addition, a concise electrical test is suggested in section 3.5 for the pre-qualification of the Athena flight detectors. The set of measurement data gained during the qualification will be the base for the spectroscopic experiments, which are described in chapter 4.

For IS chips the following issues are addressed by die-level measurements:

- Existence of short-circuits or high leakage currents.
- PMOS transistor characteristics of the DEPFET.
- NMOS transistor characteristics, also referred to as the DEPFET specific clear characteristics.

3.2. Setup for electrical qualification measurements

Prototype devices from 10 distinct wafer positions are electrically characterized for eight wafers using a probe card based setup.

3.2.1. Measurement setup

The setup for the electrical qualification measurements needs to be flexible as it is foreseen to pre-characterize all matrix sizes and formats needed for Athena with

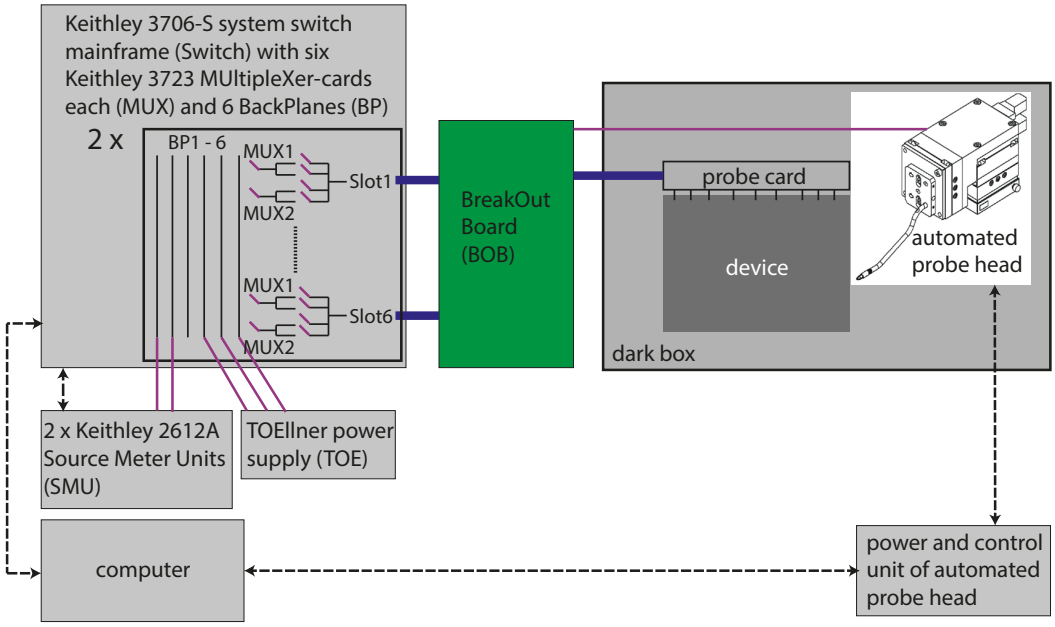


Figure 3.2.1.: Schematic drawing of the setup for electrical measurements.

the same test setup. That means, it must be extensible and in terms of efficiency it should be automatable. Therefore, a probe card based setup with an additional automated probe head and programmable mainframes is used. In contrast to bond adapters, testing with a probe card is non-destructive and reversible as the characterized dies should be integrated to full detector systems. A schematic drawing of the measurement equipment is shown in figure 3.2.1 and a photograph is provided in figure 3.2.2.

The core of the setup are two Keithley 3706-S system switch mainframes (Switches). Each of them is equipped with six high speed relay Keithley 3723 MUltipleXer-cards (MUX) providing 720 unipolar channels and six Back Planes (BP). The BP are wired to TOEllner power supply (TOE) channels and Keithley 2612A dual-channel Source Meter Unit (SMU) channels. A SMU is a four quadrant precision power supply with two precise digital multimeter channels for current and voltage sensing. The connections between BP and MUX as well as the switching of the channels are programmable and controllable remotely. All 12 MUX are coupled to the BreakOut Board (BOB) via customized 160 pin coax cables. The BOB itself is connected to the probe card via a customized 120 pin coax cable and to the automated probe head via a single pin coax cable. That means, the connections of the setup parts can be changed using the two Switches. Thus, measurements can be performed without shuffling plugs and the setup can be easily adapted to other matrix sizes and formats by using a matrix specific probe card. The whole measurement procedure including channel switching, SMU controlling and probe head movement is controlled using a single MATLAB program.

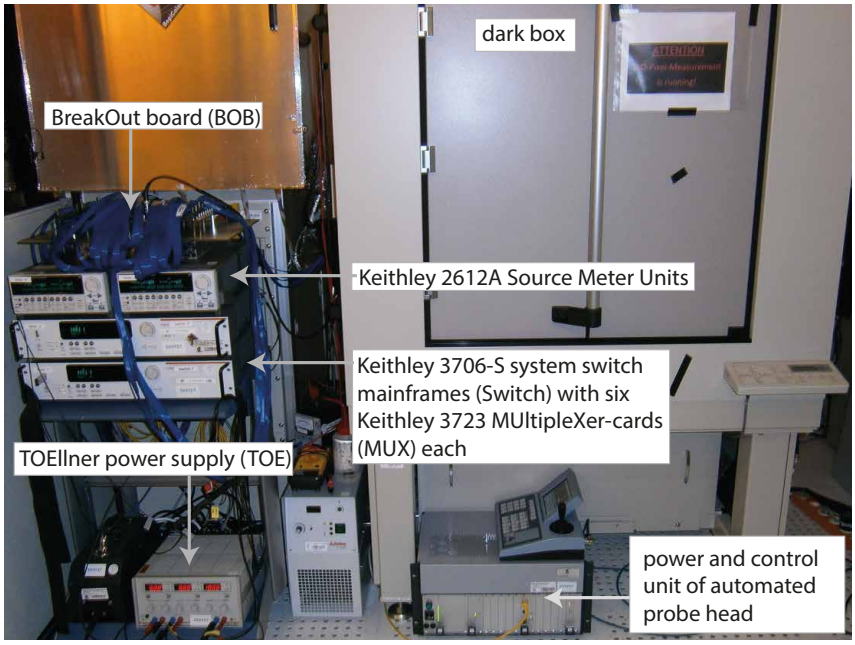


Figure 3.2.2.: The dark box of the electrical qualification setup with the belonging power supply rack and control units.

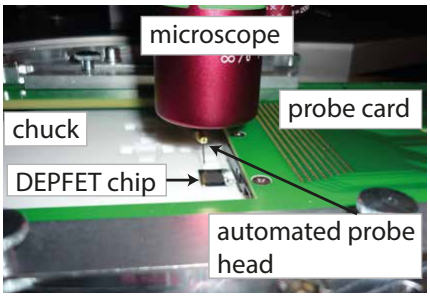


Figure 3.2.3.: Interior view of the dark box with the IS chip, chuck, probe card and automated probe head.

During the measurements the DEPFET matrix is contacted via a probe card and an automated probe head as shown in figures 3.2.3. It is placed in a customized chuck that can hold up to five devices at the same time. In order to avoid contacting the highly sensitive entrance window on the back side, the chips rest only on the non-sensitive areas at the chip edge. The devices are sucked in the chuck by negative pressure. The whole setup is located in a dark box for the purpose of avoiding light induced charge generation, which can disturb the measurements. The dark box is situated in a clean room controlled environment and the tests are performed at room temperature but under temperature-controlled conditions.

The matrix is connected as shown in figure 3.2.4. In addition to the schematic presented before in figure 2.2.13, the row-wise clear, clear gate and gate contacts are connected on-chip via bus structures to common contacts. Thus, drain, clear, clear gate and gate are biased commonly for all pixels. One column of pixels is activated

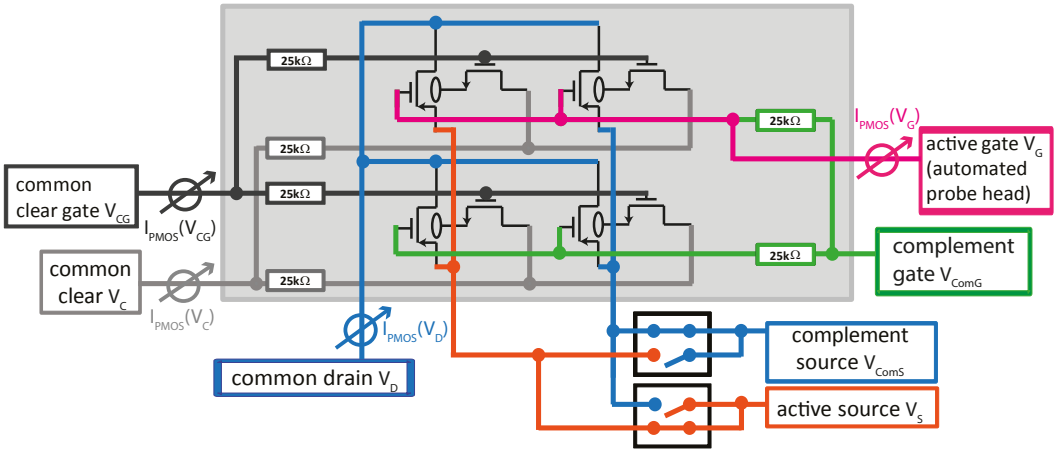


Figure 3.2.4.: Connection scheme for the electrical qualification for the example of a 2 × 2 matrix. The circuitry implemented on the DEPFET chip is indicated by the gray frame. The drain is biased as grid. Gate, clear and clear gate are biased row-wise. One column of pixels is activated via the active source. Using the active gate, a row of pixels is activated. The shown schematic is valid for all matrix sizes.

via the active source. All other columns stay at the so-called complement source potential, which is equal to the drain potential. Hence, no potential drop between source and drain exists and independent of the gate bias no transistor current is flowing. Using this connection scheme, one whole column can be measured. The automated probe head is used as active gate pulling the gate potential of just on row to on-state. All other rows stay in off state defined by the complement gate because current flow from active to complement gate is virtual inhibited with the on-chip 25 kΩ resistors. Using active source and active gate allows to address the pixels individually.

3.2.2. Measurement procedures

The electrical qualification measurements are divided into three parts:

- The first set of measurements is used for a quick leakage current test, in order to detect short-circuits.

- The second measurement is a global function test, which is in the following also referred to as column-wise test. Hence, the gate is biased commonly for all pixels without using the automated probe head. A column of 64 pixels is activated via the active source (see again figure 3.2.4). The column-wise measurements show the PMOS and NMOS characteristics of 64 transistors simultaneously.

- In contrast to the global functional test, the third set of measurements characterizes each pixel individually via an automated probe head. Here also PMOS and NMOS characteristics are measured.

Short-circuit test

The short-circuit test screens for defective matrices. This is necessary because the DEPFET matrices are single defect sensitive in terms of short-circuits within the polysilicon and aluminium layers as well as between them. During the short-circuit test routine all bias contacts (gate, clear gate, clear, drain, ring and inner substrate) are measured against each other. In addition, measurements of the source columns versus gate, clear gate and clear are performed. For a detailed contact list refer to table A.1.1 and for an overview of the biasing grid of a pixel see again figure 2.2.14. The high-port voltage is switched from 0 V to +1 V while the low-port voltage remains at 0 V. The applied potential polarity per test has to be chosen such that opening parasitic pn junctions is avoided. In the test clear versus drain e.g., the clear must be the high-port and drain the low-port as the clear contacts the n-side and drain the p-side of a pn junction. Only in this configuration the pn junction is in reverse bias.

Measurement of the transistor characteristics

When a matrix passes the short-circuit test, the transfer characteristics $I_{PMOS}(V_G)$ is measured column-wise, meaning for 64 pixels in parallel. This measurement yields the transfer characteristics of 64 PMOS transistors at the same time because in each column all pixels are biased simultaneously. During the measurements, the internal gates of the DEPFETs are held empty by applying a sufficiently positive voltage at the clear gate and the clear contacts. The gate is biased globally for all pixels without using the automated probe head. Hence, for an applied set of source V_{S}, gate V_{G} and drain V_{D} voltages the transistor current I_{PMOS} with empty internal gate can be measured. In addition, the gate is set to a potential that allows small current through the PMOS transistor, and the clear and clear gate onset for every whole column is determined. This is used as quick functional test of the transistors for all defect free prototype matrices.

	$V_D = V_{ComS}$	V_S	V_{ComG}	V_{CG}	V_C	V_G
$I_{PMOS}(V_G)$	-5 V	0 V	+5 V	+5 V	+10 V	+1.5 V$\searrow$-4.5 V
$I_{PMOS}(V_D)$	0 V$\searrow$-5.1 V	0 V	+5 V	+5 V	+10 V	$V_G(\lvert I\rvert \approx 100\ \mu A)$
$I_{PMOS}(V_{CG})$	-5 V	0 V	+5 V	+2 V$\searrow$-3.6 V	+10 V	$V_G(\lvert I\rvert \approx 50\ \mu A)$
$I_{PMOS}(V_C)$	-5 V	0 V	+5 V	+5 V	+7 V$\searrow$+0 V	$V_G(\lvert I\rvert \approx 20\ \mu A)$

Table 3.2.1.: Biasing conditions for active gate V_{G} and complement gate V_{ComG}, drain V_{D}, active source V_{S} and complement source V_{ComS}, clear V_{C} and clear gate V_{CG}. The arrow emphasizes the direction of voltage variation. The reference for all voltages is the source potential V_{S}. For $I_{PMOS}(V_D)$, $I_{PMOS}(V_{CG})$ and $I_{PMOS}(V_C)$ the active gate voltage is chosen such that at the beginning of the measurement a PMOS current $|I_{\mathrm{PMOS}}|$ of 100, 50 or 20 µA respectively is forced through the DEPFET.

In contrast to the global functional test, where always a column of 64 DEPFETs is measured at the same time, several IS matrices are tested also pixel-wise using the automated probe head as active gate, applying the biasing depicted in table 3.2.1.

Here, the transfer characteristics $I_{PMOS}(V_G)$, the output characteristics $I_{PMOS}(V_D)$ and the DEPFET specific clear $I_{PMOS}(V_C)$ and clear gate characteristics $I_{PMOS}(V_{CG})$ are measured.

Measurement timing and precision

The timing of all measurements is chosen such that quasi-static conditions are ensured. Therefore, three main delay times are set in the test routines to guarantee that the setup and device have settled in equilibrium after changing connections and voltages:

- time after changing MUX-to-BP connections in the Switches i.e. the transition from transfer characteristics measurement to clear characteristics test. Changing such connections needs a delay of about 0.5 s.
- time after closing or opening channels of the MUX i.e. selection of another column of pixels with the active source requires about 0.00005 s.
- time after changing applied voltages with the SMU i.e. allowing for settling of conditions for the new measurement step. This delay varies within the DEPFET designs and is in the order of magnitude of 0.001 s.

These delays must be adapted for all four DEPFET designs as well as for every measurement procedure. The delay times also differ slightly between column-wise and pixel-wise measurements. Hence, it is tested for all measurements whether the speed per measuring point needs to be extended or whether it can be shortened and still gives reliable results. Therefore, with the four DEPFET designs all measurement routines have been performed with increasing delays for the first row and column of the matrix. The gained measurement data sets are compared within design and measurement procedure. If no difference between routines with different delays is noticed, the shortest delay will be taken. The measurement time for one whole matrix using the column-wise test is about 30 minutes. For pixel-wise measurements, the measurement time extends to number of rows multiplied by 30 minutes. This results in our case in about 32 hours per die containing 64×64 DEPFETs.

In order to ensure correct measurements, a short-circuit test between all needles of the probe card is performed before the touchdown onto the die. By applying a voltage difference of 1 V between two needles, it can be tested whether short-circuits caused by dust particles exist. In case of the absence of short-circuits, the measured current is the open-loop current of the setup. The metering precision is defined as the maximum value of this current. The open loop current of the setup is found to be 0.5 nA.

The measurement accuracy of the qualification setup results from the used SMU and TOE power supply. The sourcing accuracy of both supplies is given as 0.02%. The sensing accuracy of the Keithley 2612A SMU is specified in the data sheet and shown in table 3.2.2.

In figure 3.2.5 a representative transfer characteristics of the cut gate design is shown. The error bars per data point represent the actual measurement error. Just for the

range	accuracy
100.0 nA	± 0.06% + 100 pA
1.0 µA	± 0.025% + 500 pA
10.0 µA	± 0.025% + 1.5 nA
100.0 µA	± 0.02% + 25 nA
1.0 mA	± 0.02% + 200 nA
2 V	± 0.02% + 350 µV
20 V	± 0.015% + 5 mV

Table 3.2.2.: Sensing accuracy of the Keithley 2612A SMU

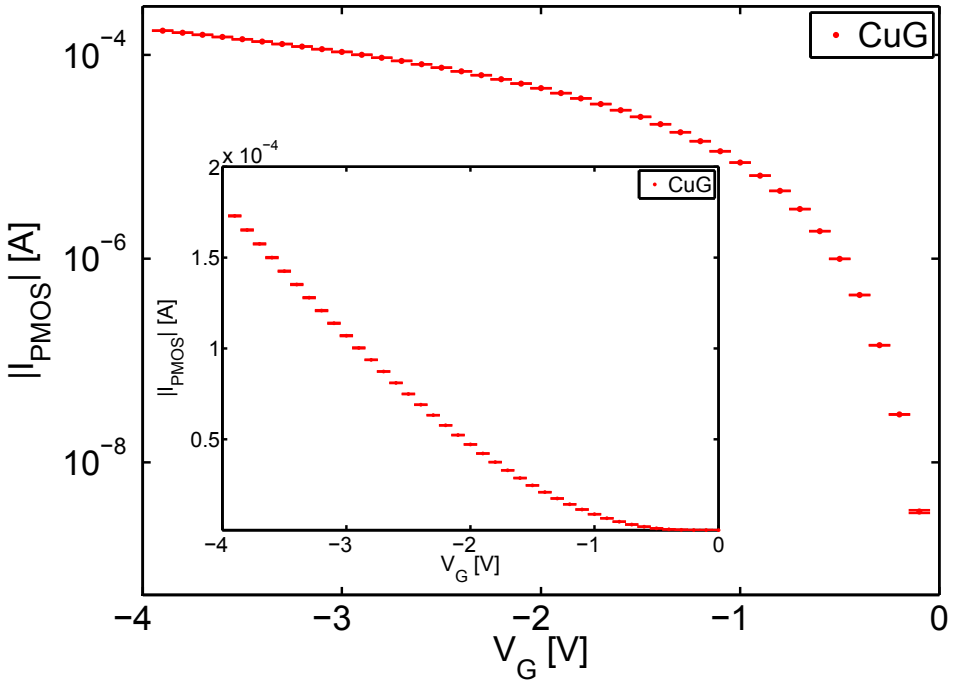


Figure 3.2.5.: The transfer characteristics of one representative pixel for the cut gate (CuG) design including the measurement error per data point. The inset shows the same curve with linear scaling. The error bar is always smaller than the data marker.

measurement point (-0.1 V, 3.3 nA) the error bar has a visible length. The errors are three orders of magnitude smaller than the measurement data and thus are neglectable. In the following sections no error bars will be shown in the measurement graphs. For every characteristic value, which are discussed in the results section 3.3, the fluctuation among the pixels of one device are significantly larger than the measurement errors. Hence, either the standard deviation or the full width per die of the characteristic values are given.

3.3. Results of the electrical qualification

In this section, the results of the electrical qualification of the four different DEPFET designs, see again figure 2.3.1, are presented. First of all, the yield gained from the short-circuit tests is shown. Afterwards the results for the transfer characteristics from the column-wise measurements are compared to those from the single pixel measurements. Then the pixel-wise output characteristics as well as clear and clear gate characteristics are presented.

3.3.1. Yield of the IS devices

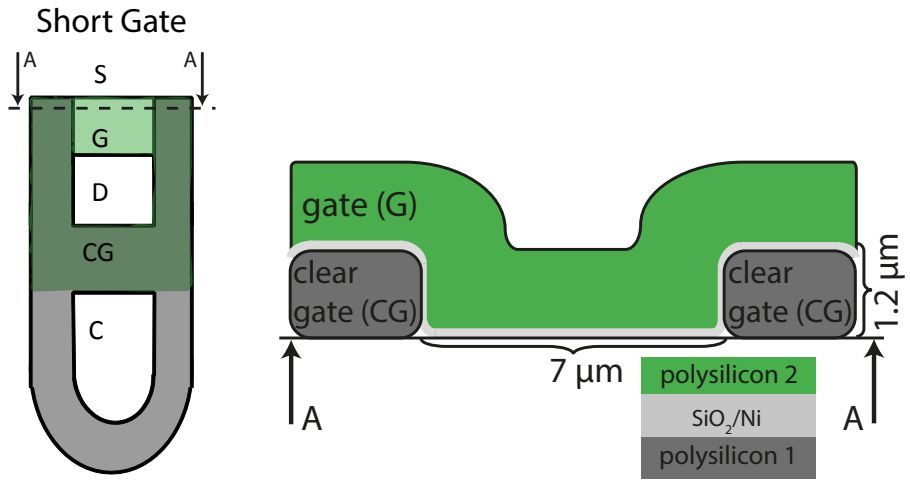
10 prototype devices from eight wafers, which have been produced in two batches, were tested for short-circuits. 70 out of in total 80 prototype matrices were found to be short-circuit free. An overview of the production yield for the two batches is given in table 3.3.1. No systematic difference in the yield of the two production batches was found. The production yield for the IS matrices is 88%. Applying this to the chip area gives in average 1 defect per 10 cm^2.

	30	31	32	33	34	35	36	37
E01 (Quasi Linear)			*	o		o	o	
E02 (Cut Gate)						o		
F01 (Narrow Gate)						o	o	
F02 (Narrow Gate)						o		
F19 (Cut Gate)						o		
F20 (Cut Gate)						o		
G19 (Narrow Gate)						o	o	
G20 (Cut Gate)		o				o	o	
J19 (Short Gate)						o	o	
J20 (Cut Gate)						o		

Table 3.3.1.: Rating for the short-circuit measurements of the eight wafers on die-level. gray wafer numbers: produced in batch two; red: defect; green: O.K.; * damaged accidentally during test; o are tested pixel-wise with the automated probe head additionally to the column-wise testing.

Upon a closer view in table 3.3.1 can be seen that the short gate devices are most likely to show short-circuits. For structure J19 of wafers 31 and 33 it is very probable that the defects are short-circuits between the two polysilicon layers. Figure 3.3.1 shows a schematic drawing of the crucial area of the short gate design, which cannot be found in the other designs in this form. During the deposition and structuring of the isolator and polysilicon layer 2 on top of polysilicon layer 1, the gate area is susceptible to develop short-circuits between the polysilicon layers [53]. As wafer 31 has been produced with an isolator between the polysilicon layers that is 30 nm thicker than that of wafer 33, improving the isolator does not appear to solve this issue. For the short gate design a layout relaxation is suggested by either reducing

the polysilicon 1 structure height or by increasing the channel length. For device J19 of wafers 30 and 34 several defects are recognized including short-circuits between the polysilicon layers and within the aluminium layers. A more detailed prediction is not possible with the used measurement procedure because only non-consistent measurement data for the wafer level tests have been provided due to the production schedule in advance of this thesis. Removing all J19 from the statistics would increase the yield to 1 defect per 17.5 cm^2.



(a) Short gate with cut.

(b) Scheme of the cut section through gate and clear gate of the short gate design.

Figure 3.3.1.: The critical area in the short gate design processing is the gate region. There the polysilicon 2 must climb two times over the stack of polysilicon 1 and the isolator with a height of 1.2 µm within a distance of 7 µm.

For the cut gate structures E02 of wafer 37 and F20 of wafer 36 also short-circuits between the two polysilicon layers were measured. For all designs despite the short gate an increase of the isolator about 30 nm is helpful because this again increases the breakdown voltage between the polysilicon layers from 35 V to 94 V. As mentioned before, wafer 30 and 31 are processed this way and do not show this failure despite the short gate devices. Using a thicker nitride layer between the polysilicon structures is known to decrease the radiation hardness of the DEPFET [54] and it must be simulated whether this preventive action is needed for Athena.

Other crucial production steps, which can cause short-circuits, are the deposition and etching of the aluminium wiring and the isolator layer because of hillock formation owing to electromigration in thin films [55]. These spherical surface protrusions grow at grains of the aluminium layer during annealing processes because of differences in the thermal expansion coefficient between film and substrate [56, 57, 58]. If a voltage difference is then applied to the aluminium wire, electric field peaks would occur at hillocks and this can cause short-circuits. This kind of defect was found for five IS devices.

In order to reach a defect free chip area of about 54 cm^2, which would be necessary for one 448 $\times$ 640 pixel Athena chip, the yield must be increased. Thus, the aluminium processing is for example being improved by a treatment with hot de-ionized water, as proposed in [59], for newer productions. In addition, an improvement of the inter-metal-isolator is suggested as well as one defreckle etching step after every aluminium deposition step when using a sputter target that contains silicon.

All 70 defect free matrices, which are marked green in table 3.3.1, are characterized column-wise and, in addition, a representative sample of 17 matrices, which is marked with o in table 3.3.1, is characterized pixel-wise. The sample is chosen such that all chips of the defect free wafer 35, every design from a wafer of another production batch, here wafer 36, and spot checks of two additional wafers are included.

3.3.2. Transfer characteristics

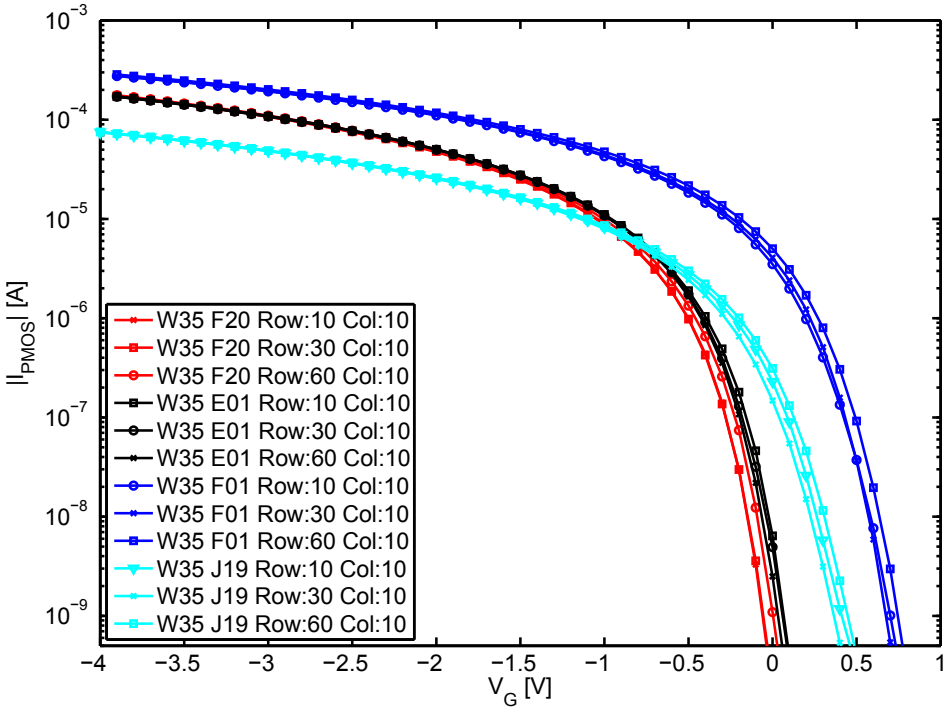


Figure 3.3.2.: The transfer characteristics of several pixels from devices F20 (cut gate), E01 (quasi linear), F01 (narrow gate) and J19 (short gate) from wafer 35.

In figure 3.3.2 the transfer characteristics of several pixels from devices F20, E01, F01 and J19 from wafer 35 are shown. These devices have been chosen as representatives of the four DEPFET designs. It can be seen, that the characteristics group with design type, which are mirrored with the four colors in the graph. This leads to the conclusion, that the characteristics of the pixels of one chip are different in their absolute measured values but similar in curve shape. Furthermore, the deviation within a device does not overlay the difference between the DEPFET variants. In order to show parameter extraction points and discuss differences among the DEPFET designs in the following sections, the characteristics of the pixel in row 10 and column

10 from devices F20 (cut gate), E01 (quasi linear), F01 (narrow gate) and J19 (short gate) from wafer 35 are used as representatives and are referred to as typical data set. The inter-pixel variation for the devices is given for the extracted parameter as the full width per die.

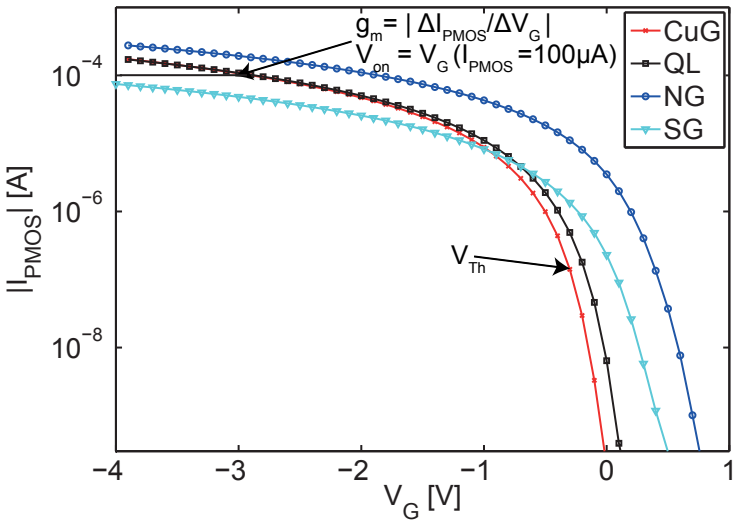


Figure 3.3.3.: The transfer characteristics of one representative pixel for each design from wafer 35: QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate. For the cut gate (CuG) curve the parameter extraction points for the defined gate on voltage V_{On} and the transconductance g_{m} as well as the threshold voltage V_{Th} are marked.

The typical data set of the pixel-wise measured transfer characteristics for the four DEPFET variants is depicted in figure 3.3.3. As expected from the transistor current equation 2.2.18, the curve shapes vary depending on the relation of gate width W to length L of the design variants. In order to compare the DEPFET designs, a set of transistor characterization parameters is extracted from the transfer characteristic measurements for every device. The first parameter extracted from the transfer characteristics is the threshold voltage V_{Th} because following equation 2.2.16, it gives information about the general physics in the transistor channel. The parameter set includes also the gate voltage for the defined on-state $V_{On} = V_G(|I| = 100\ \mu A)$. For the spectroscopic measurements in chapter 4, the DEPFET is operated in the saturation region with a transistor current $|I_{\mathrm{PMOS}}|$ of 100 µA. V_{On} gives information about the voltage variation between the pixels within a matrix needed to reach the same I_{PMOS}. This variation depends on the production technology and shows how the DEPFET design impacts the reached production homogeneity. At the operational point used for the spectroscopic characterization also the transconductance g_{m} is extracted from the transfer characteristics. According to equation 2.2.34, g_{m} defines the detector gain together with g_{q}.

As mentioned in section 3.2.2 and 3.3.1, before a representative sample of devices is characterized pixel-wise, all defect free IS chips are measured column-wise. For

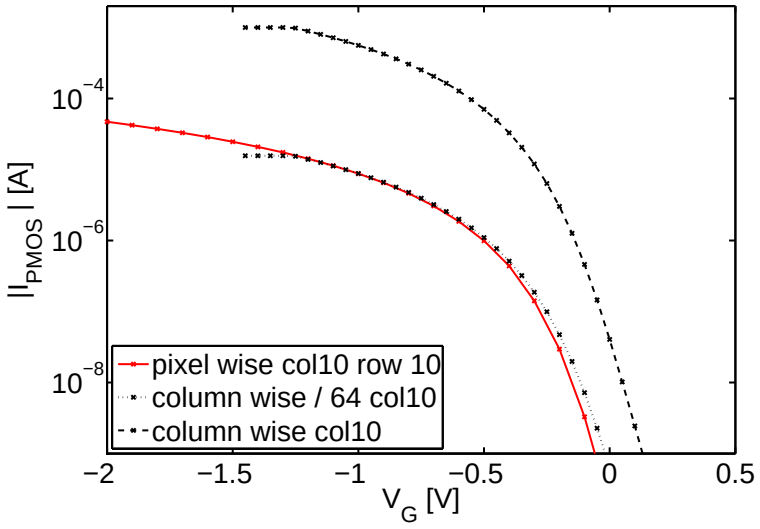


Figure 3.3.4.: Comparison of the column and pixel-wise measured transfer characteristics of a cut gate (CuG) device. The flat in the column-wise curves results from the current limitation of the measurement setup.

the measurement of 64 PMOS transistors in parallel the same parameters are extracted as for the single pixel characterization but they are indicated with 64 in the symbol, e.g. V_{Th64}. A comparison between these measurements is valid because the pixel-wise curve is similar to the column-wise curve divided by 64, as evidenced in figure 3.3.4. The transfer characteristics of a single pixel from column 10 is just similar and not identical to the column-wise characteristics, which is divided by 64, because the column-wise measurement contains the sum of 64 pixel deviations, see again figure 3.3.2. It must be also considered that the two measurements have been performed with a time difference of several weeks. In addition the measurement temperature may be higher for the column-wise measurement as the IS chips are not cooled or temperature controlled during the electrical tests. In the following the results for V_{Th64} will be shown first followed by V_{Th}.

Threshold voltage

An important parameter of the transfer characteristics is the threshold voltage. It is always extracted from I_{PMOS} (V_{G}) measurements with empty internal gate, hence the clear and clear gate are kept in on-state during the measurement. The threshold voltage V_{Th} can be measured for individual pixels or indicated with V_{Th64} for one whole column, when I_{PMOS} is measured for 64 pixels in parallel as described in section 3.2.2, respectively. The DEPFET is operated in saturation, as will be explained in section 4.3, and therefore only two methods for extracting the threshold voltage of a transistor remain out of more than ten [60]:

- Extrapolation method in the Saturation Region (ESR): linear extrapolation at the maximum slope of the $\sqrt{|I_{\mathrm{PMOS}}|}(V_{\mathrm{G}})$ function. The intersection of the linear extrapolation with the x-axis marks V_{Th} or V_{Th64}, respectively.

- G1 function method: linear extrapolation of the G1(V_G,I_{PMOS}) function derived in [61, 62].

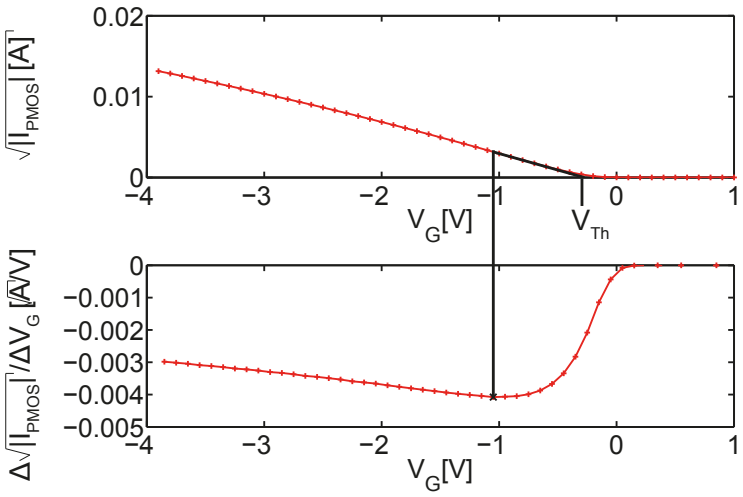


Figure 3.3.5.: The determination of the threshold voltage V_{Th} using Extrapolation method in the Saturation Region (ESR) for the pixel-wise cut gate (CuG) characteristics from figure 3.3.3. The graph on the top shows the measured transfer characteristics as $\sqrt{|I_{PMOS}|}(V_G)$ function. The graph on the bottom shows its slope. At its maximum slope, $\sqrt{|I_{PMOS}|}(V_G)$ is extrapolated linearly. The intersection of the extrapolation with the x-axis marks V_{Th}.

The two threshold voltage extraction methods are applied to all devices in order to compare their results for column and pixel-wise measurements. The two methods give nearly the same results, see section A.1.2 for more information. The Extrapolation method in the Saturation Region (ESR) seems more reliable because for the G1 function method it is unclear in the literature where exactly the function should be linearly extrapolated. So ESR is the method of choice for extracting the threshold voltage of the DEPFET. The extraction method in the saturation region is displayed in figure 3.3.5. At the point of its maximum slope, the $\sqrt{|I_{PMOS}|}(V_G)$ function is extrapolated linearly. The threshold voltage V_{Th} equals the intersection of the linear extrapolation with the x-axis.

In figure 3.3.6 the mean value of V_{Th64} per device is depicted. The standard deviation σ of V_{Th64} for every device is below 0.05 V. V_{Th64} is shifted up to 1.2 V to more positive voltages for narrow gate and short gate devices (F02, F01, G19, J19) with respect to quasi linear and cut gate structures. It can be seen that the devices group with design and no systematic difference between the wafers is found. The graph shows also that V_{Th64} for drain readout matrices deviates to V_{Th64} for source follower devices.

This is no intrinsic effect of the structures. It is due to the measurement routines used for the column-wise measurements that applies the negative V_D potential at the global contact. In case of the drain readout devices, V_D is applied at the source contact, which surrounds the gate. A comparison of global threshold voltages V_{Th64}

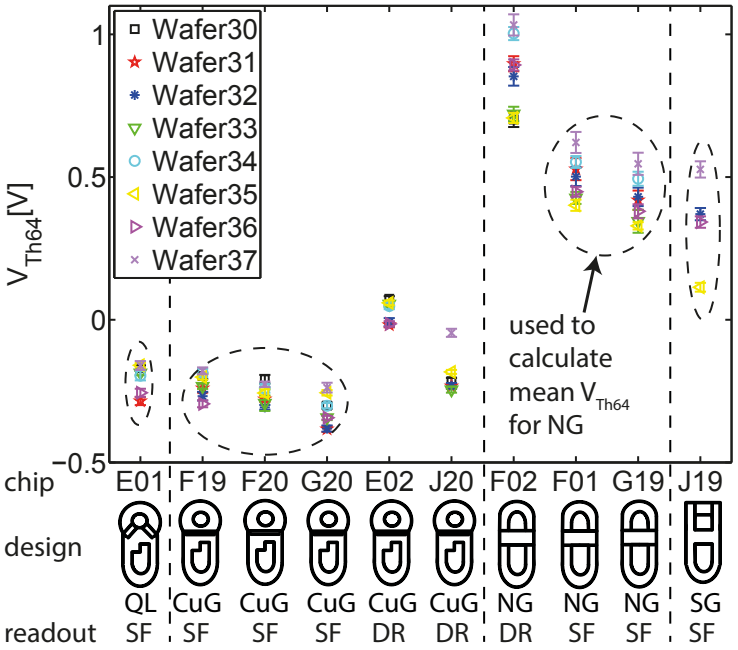


Figure 3.3.6.: Mean of V_{Th64} for all 70 defect free devices. The plotted error bar represents the standard deviation σ of V_{Th64} between the columns for every device. For most devices the error bar is smaller than the symbol. The dashed ellipses marks the devices per design that are summarized for comparison in tables 3.3.3.

measured for normal and interchanged source and drain potential is shown in figure 3.3.7. It can be seen clearly that when the drain readout devices are biased with 0 V at the global contact, which is the source, the threshold shifts (blue arrows) closer to the source follower devices of their design group. The same is true for source follower chips in reverse (red arrows). In order to compare drain readout and source follower devices, only the blue marked V_{Th64} in figure 3.3.7 are used. For the mean parameter values per design group just source follower devices are summarized for the column-wise measurements, which are shown in figure 3.3.6 and table 3.3.2, as the inverse measurements have been done only for devices of wafer 35.

Design	**Possible chips**	**Sample size**
quasi linear (QL)	E01	7
cut gate (CuG)	F19, F20, G20	23
narrow gate (NG)	F01, G19	15
short gate (SG)	J19	4

Table 3.3.2.: According to the availability of the DEPFET designs, see table 3.3.1, and the restriction through applied voltages of the measurement routines, the statistic sample size of the variants for column-wise measurements is presented.

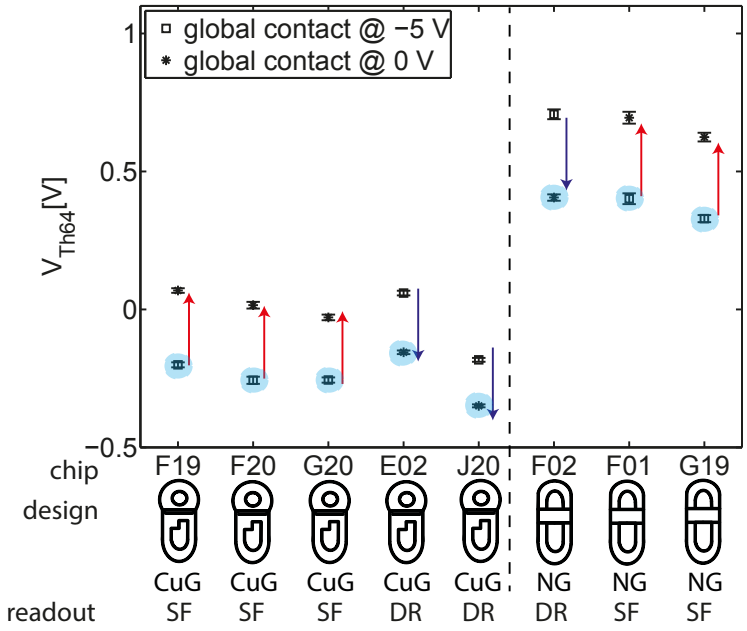


Figure 3.3.7.: Mean V_{Th64} for all cut gate (CuG) and narrow gate (NG) devices of wafer 35 for the normal and the inverse measured transfer characteristic. The error bars represent σ within every device. Blue arrow = drain readout device shift for inverse measurement, red arrow = source follower device shift for inverse measurement, blue mark = comparable biasing for source follower and drain readout.

Table 3.3.3 shows the difference in V_{Th64} from quasi linear or cut gate devices compared to narrow gate or short gate devices like figure 3.3.6 does. The maximum shift is 0.74 V because the inverse biased drain readout devices are excluded from the summary as they would distort the results.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}
V_{Th64} $[V]$	-0.27	0.06	-0.20	0.05	+0.46	0.08	+0.34	0.17

Table 3.3.3.: Mean threshold voltages for the column-wise transfer characteristics are summarized according to table 3.3.2 for each design. Mean σ is the average standard deviation per die.

To gain more information about the voltage shift for interchanged potential of the global contact, cylindrical simulations were done using TeSCA as described in section 2.4. For these simulations, again the cut section through the PMOS of the cut gate design in source follower configuration, as shown before in figure 2.4.1, is used. Hence, the drain contact in the center of the gate is the global contact and the source is connected column-wise. Potential plots of the simulation data applying -5 V and 0 V to the source and drain contacts are presented in figure 3.3.8. In order to inhibit a current flow from source to drain, the gate is set to its off-state with +5 V in both cases. As the backside is not contacted during the electrical characterization measurements, V_{B} is set to 0 V for the simulation.

The depletion region below the gate is shifted more towards the drain in figure 3.3.8b compared to figure 3.3.8a. This shift results from the geometry of the DEPFET that has been shown before in figure 2.4.1. Drain, gate and source form a cylindrical capacitor with a potential, which does not change linearly with the radius between the two p-doped areas. In addition, the potential drop between source and drain is lower when -5 V are applied to the source contact due to the space charge effect of the larger source contact. Both effects lead to a lower barrier between the p-doped regions of the transistor. Even if the PMOS transistor is turned off, holes will diffuse below the gate. More holes are attracted if a more positive gate potential is applied, therefore the transistor channel is formed for more positive gate voltages. Thus, the threshold voltages V_{Th64} are shifted to more positive gate voltages V_{G}.

In order to compare the column-wise determined V_{Th64} for all devices of wafer 35 to the pixel-wise V_{Th}, the measurements of the column-wise transfer characteristics with the global contact at 0 V is taken for the drain readout devices and with the global contact at -5 V for the source follower configuration respectively. In figure 3.3.9 can be seen that the threshold voltages obtained with the pixel-wise and the column-wise measurement method are similar to each other. V_{Th64} is for all matrices slightly more positive than V_{Th} because V_{Th64} is determined without dividing the column-wise measurement by 64. This could be seen in figure 3.3.4.

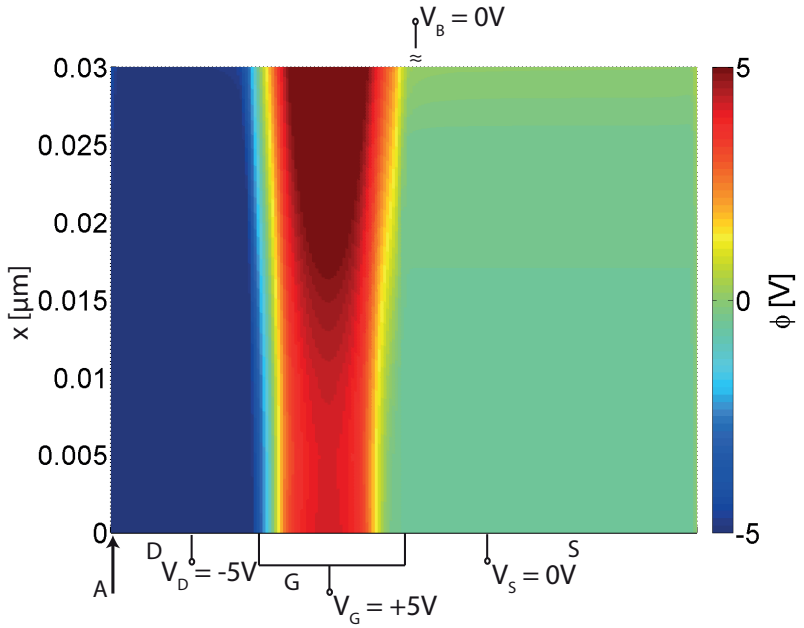
Design	**Possible chips**	**Sample size**
quasi linear (QL)	E01	3
cut gate (CuG)	E02, F19, F20, G20, J20	7
narrow gate (NG)	F01, F02, G19	5
short gate (SG)	J19	2

Table 3.3.4.: According to the availability of the DEPFET designs, see table 3.3.1, and the chosen sample restrictions mentioned in section 3.3.1, the statistic sample size of the variants for pixel-wise measurements is presented.

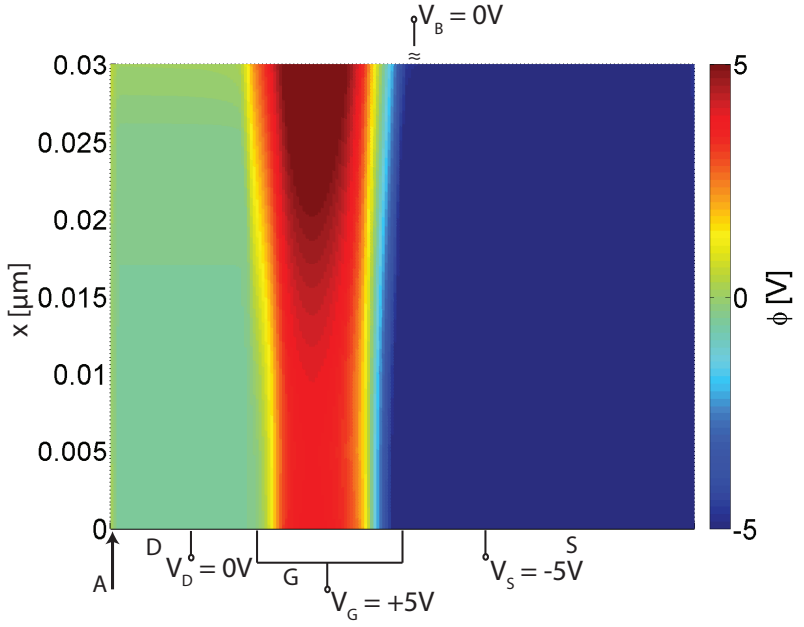
Figure 3.3.10 presents the average threshold voltage V_{Th} for all IS devices that have been characterized pixel-wise. In contrast to figure 3.3.6, here the error bar represents the full width of the parameter per die

$$\Delta_{\mathrm{Die}} = \max(V_{\mathrm{th}}) - \min(V_{\mathrm{th}})$$

For the column-wise measurement, V_{Th64} is already an average value. Thus, the full width can not be determined and giving the standard deviation σ is appropriate. For the pixel-wise characterization on the other hand, Δ_{Die} can be calculated and shows the parameter width with that the steering and readout ASICs must cope. The devices within one dashed line in figure 3.3.10 are summarized for the comparison of the designs in table 3.3.5. For the pixel-wise characterization the summary of source follower and drain readout configuration per design is possible as shown in figure 3.3.10. The resulting sample size is listed in table 3.3.4 and the average parameter value is given in table 3.3.5.



(a) Normal bias: -5 V applied at the smaller drain and 0 V at the source.



(b) Inverse bias: 0 V applied at the smaller drain and -5 V at the source.

Figure 3.3.8.: Potential plots for the cross section through drain (D), gate (G) and source (S) of the cut gate (CuG) design in source follower (SF) configuration, as used before in figure 2.4.1, with external bias. The gate is turned off with +5 V. The potential drop is higher below the gate (G) for the inverse bias and it is shifted towards the drain (D) contact owing to the space charge effect of the larger source (S) contact.

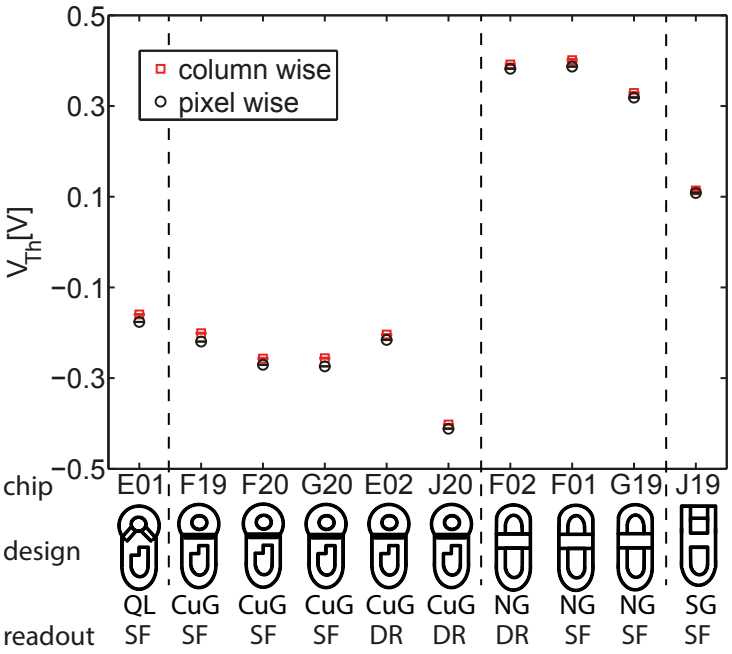


Figure 3.3.9.: Comparison of threshold voltage between pixel and column-wise measurements obtained for all devices of wafer 35. The source (S) is set to 0 V and the drain to -5 V for all measurements.

In case of the single pixel characterized dies also no systematic differences among wafers are visible and the devices group with design as shown in figure 3.3.10. The threshold voltages V_{Th} of narrow gate and short gate structures are shifted up to 0.7 V to more positive gate voltages as seen for the column-wise measurements. Considering equation 2.2.16

$$V_{\mathrm{Th}} = \Phi_{\mathrm{MS}} + \Phi_{\mathrm{Ox}} + 2\Phi_{\mathrm{F}} - \frac{\sqrt{2\epsilon_{\mathrm{Si}}\epsilon_0 q N_{\mathrm{D}}(2\Phi_{\mathrm{F}} - V_{\mathrm{SB}})}}{C'_{\mathrm{G}}}$$

all designs should have the same threshold voltage V_{Th} because the used doping rate (concerning Φ_{F}, V_{SB} and N_{D}) as well as the MOS structure (concerning ϵ_{Si}, C'_{G}, Φ_{MS} and Φ_{Ox}) are supposed as equal among all devices. The possible influence of the gate design on the doping rate is neglected because guessing its amount is not useful without the support of three dimensional simulations. Though a threshold voltage shift is likely to occur for short channel devices. A transistor is considered to have a short channel when the gate length L is in the order of magnitude of the depletion depth of the biased pn junctions of source and drain [38]. This is true for L of all four DEPFET designs investigated in this thesis.

Short channel effects like the threshold voltage shift can be explained by different models. A schematic drawing of a short and a long channel transistor with the coordinating abstractions as ideal transistors is shown in figure 3.3.11. The charge sheet approximation used in [28] states e.g. that the charge in the depletion region below the transistor channel is shared between the gate capacitor and the pn junctions, see figure 3.3.11a. For a transistor with short L, not every ionized donor atom of the

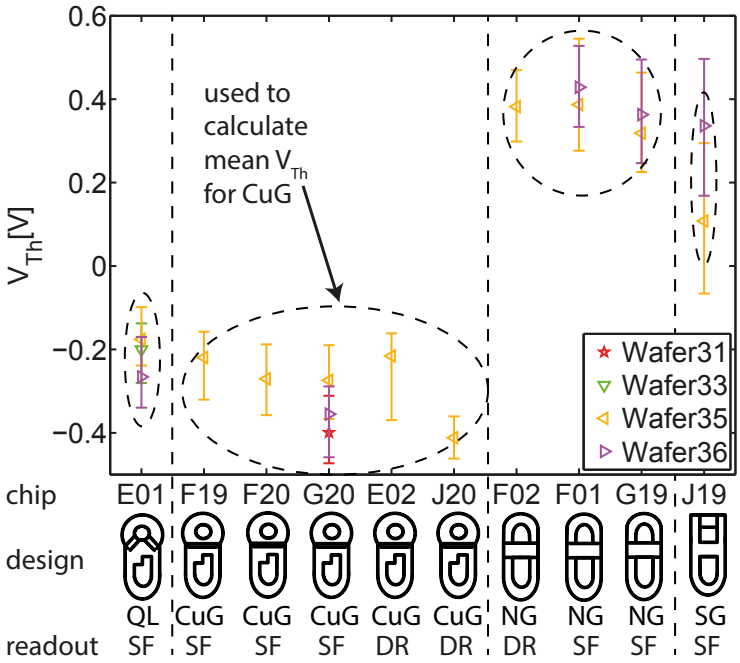
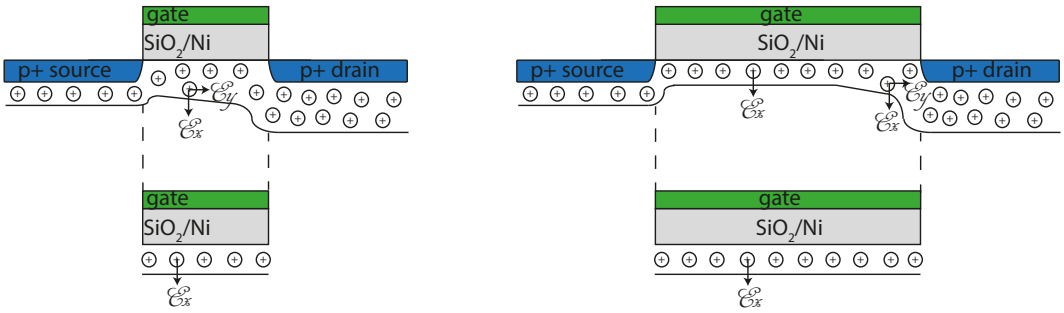


Figure 3.3.10.: Average threshold voltage V_{Th} for the 17 pixel-wise characterized IS devices. The error bar represents the full width per die. For the comparison of the designs in table 3.3.5, the chips within the dashed ellipses are summarized.



(a) Short channel PMOS transistor abstraction as ideal transistor.

(b) Long channel PMOS transistor abstraction as ideal transistor.

Figure 3.3.11.: Top half: schematics of the realistic form of the transistor channel. Bottom half: formalizing abstraction of the transistor channel. For short channel transistors the formalizing abstraction according to the equations from section 2.2.2 are not representative as the edge effects caused by the pn junctions are larger than the ideal region.

depletion layer is mirrored as electron on the gate because of the impact of source and drain pn junctions. The same gate bias V_{G} for the short and the long channel device leads to the same amount of electrons on the gate capacitor for both structures. But for the short transistor more of the electrons are left for being mirrored into the inversion layer instead of the depletion layer. Thus, a higher current flow is possible in the shorter channel for the same V_{G}.

For the explanation of the existence of short channel effects in devices with unknown channel doping profile, the electrical field $\mathcal{E}$ can be used instead [63]. In the ideal transistor in most channel elements only the vertical component of the electrical field $\mathcal{E}_x$ is dominant as shown in figure 3.3.11b. Thus, the Poisson equation 2.2.22 is just one-dimensional. For short channel structures the horizontal component must be added and the Poisson equation is just solvable numerically. Owing to its complex three dimensional structure, the DEPFET cannot be mapped with neither the ideal transistor equations nor existing models for short channel transistors as even for linear transistor geometries numerical calculations are not exact and case specific [38, 64].

Summarizing, the differences in V_{Th} among the DEPFET designs is evidence for the presence of short channel effects. This leads to an impact of the gate, drain and source dimensions on the threshold voltage. The full width of V_{Th} per die is up to twice that of quasi linear and cut gate dies for short gate and narrow gate devices. Owing to the smaller gate dimension of the short gate and narrow gate designs, variations during the etching process of the gate polysilicon have a greater impact on the behavior of the dominance of the short channel effects compared to quasi linear or cut gate designs.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}
V_{Th} $[V]$	-0.31	0.16	-0.21	0.15	+0.38	0.22	+0.22	0.34

Table 3.3.5.: Average threshold voltages V_{Th} for the DEPFET design groups according to table 3.3.4. Mean Δ_{Die} is the average full width of the parameter per die.

For all of the following transistor parameters the results of the column-wise and pixel-wise measurement methods are similar, too. Hence, only the pixel-wise results are discussed in the main section because they provide more detailed information about the homogeneity within a device. The parameters extracted from the column-wise measurements are provided in the appendix starting at A.1.3. The statistically relevant sample size for the column and pixel-wise characterization listed in table 3.3.2 and 3.3.4 respectively are also valid for the transistor parameters given in the result tables in the following sections.

Gate voltage for the defined on-state of the PMOS transistor

Another parameter that can be extracted from the transfer characteristics of the DEPFET measured with empty internal gate is V_{On}. For this voltage a transistor current $|I_{\mathrm{PMOS}}|$ of 100 µA, which is defined as I_{On}, flows through one pixel of the matrix. It represents the gate voltage for the nominal on-state of the PMOS transistor and it is determined by linear interpolation of the neighboring measurement points of I_{On}.

As presented in figure 3.3.12 and table 3.3.6, for short gate devices a more negative gate voltage V_{On} must be applied to reach the on-state of the transistor than for

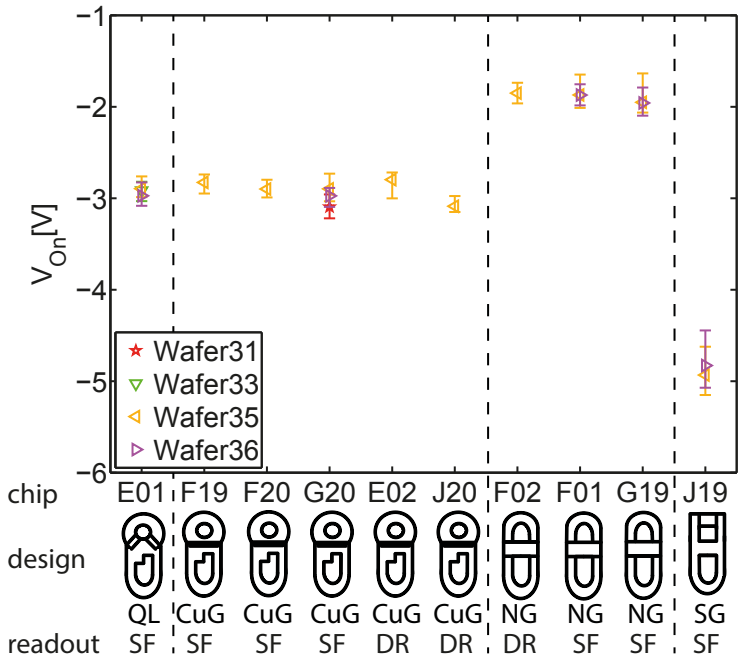


Figure 3.3.12.: Average gate voltage for the defined on-state $V_{On} = V_G(|I| = 100\ \mu A)$ of the PMOS transistor. The error bar marks the full width per die for the 17 pixel-wise characterized IS devices.

the nearly circular cut gate and quasi linear designs. Despite of their positive V_{Th}, the short gate structures have with 2.41 (see table 2.3.1) the lowest $\frac{W}{L}$, which is according to equations 2.2.17 and 2.2.18 crucial for i.e. the transconductance g_{m}. The narrow gate devices have a positive V_{Th} and with 8.97 the highest $\frac{W}{L}$. Thus, they reach their on-state for the most positive gate voltage, which matches the transfer characteristics displayed earlier in figure 3.3.3. As well as for V_{Th}, the full width per die of V_{On} increases with decreasing gate dimensions.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}
V_{On} [V]	-2.92	0.23	-2.93	0.23	-1.89	0.31	-4.88	0.58

Table 3.3.6.: Mean gate on voltages V_{On} determined for the transfer characteristics over all single pixel characterized chips from every DEPFET design. Mean Δ_{Die} is the average full width of the parameter per die.

Transconductance

The transconductance g_{m} of the PMOS is also determined at a transistor current $|I_{\mathrm{PMOS}}|$ of 100 µA. According to equation 2.2.20, it is the slope of the transfer characteristics. The resulting transconductance values are presented in table 3.3.7 and in figure 3.3.13.

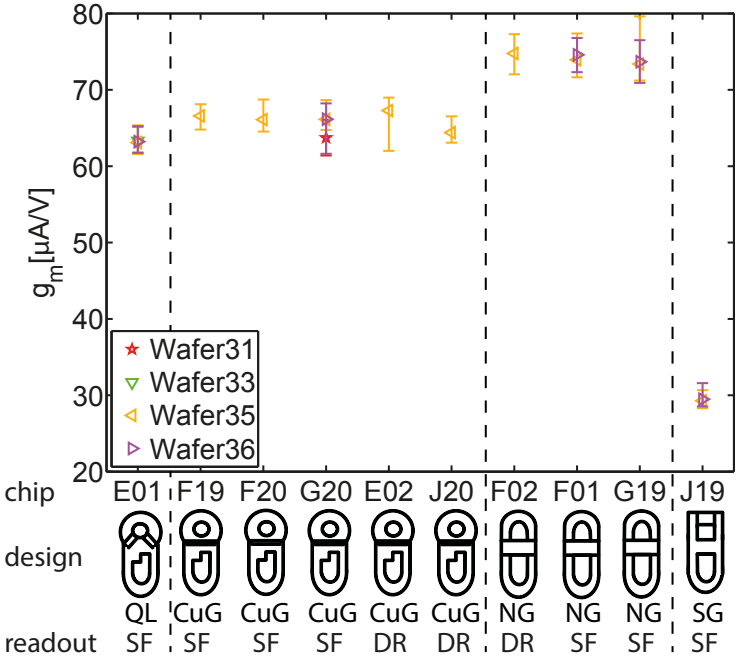


Figure 3.3.13.: Mean transconductance g_{m} of the PMOS transistor at the defined on-state $V_{On} = V_G(|I| = 100\ \mu A)$ for the pixel-wise characterized sample devices. The error bar represents the full parameter width per die.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}
g_m $[\mu A/V]$	65.8	4.7	63.2	3.6	74.0	5.9	29.4	2.7

Table 3.3.7.: Average transconductance g_{m} determined at $V_{On} = V_G(|I| = 100\ \mu A)$ for the transfer characteristics over the pixel-wise characterized sample size for every DEPFET design. Mean Δ_{Die} is the average full width of the parameter per die.

According to equation 2.2.20, the PMOS transconductance depends on:

- the applied voltages V_{GS} and V_{DS}.
- the charge carrier mobility in the channel μ_{P}.
- the gate oxide capacitance C'_{G}.
- the relation between gate width and length $\frac{W}{L}$.

For the DEPFET design variations in this thesis, μ_{P} is considered as constant due to the identical production steps and the same materials used for all wafers of the two production batches. A V_{DS} of -5 V is applied throughout all measurement routines. The only changing parameters are the ratio of gate width to length $\frac{W}{L}$, presented in table 2.3.1 as well as C'_{G} for wafers 30 and 31. Instead of a nitride layer thickness d_{Ni} of 30 nm, a thickness of 60 nm has been used for the two wafers resulting in a C'_{G} of $1.62 \cdot 10^{-4}\ \frac{\mathrm{F}}{\mathrm{m}^2}$ instead of $1.76 \cdot 10^{-4}\ \frac{\mathrm{F}}{\mathrm{m}^2}$ determined in section 2.2.2 for the other wafers.

As expected from the ratio of gate width to length $\frac{W}{L}$, the devices range with design type. With about 29.4 $\frac{\mu A}{V}$, the short gate structures show the lowest g_m, while with about 74 $\frac{\mu A}{V}$ the narrow gate structures show the highest g_m. Quasi linear (QL) and cut gate structures lie in between with about 65.8 $\frac{\mu A}{V}$ and 63.2 $\frac{\mu A}{V}$ respectively. The cut gate device G20 from wafer 31 has with 63.7 $\frac{\mu A}{V}$ a lower g_m than those G20 dies from wafers 35 and 36 with 66.1 $\frac{\mu A}{V}$. This is the result of the thicker nitride layer in the gate MOS structure. According to equation 2.2.20, increasing the nitride layer and thus lowering C'_G, results in a lower g_m. A quantitative comparison of the g_m values with the prediction of the formula is not possible owing to the presence of short channel effects and the non-linearity of the DEPFET structures. A similar arrangement of the devices is depicted in figure A.1.3 in the appendix for g_{m64}. As described in equation 2.2.34, the intrinsic amplification results from the ratio of g_q to g_m. Thus, lowering g_m will increase the DEPFET gain g_d, if g_q is assumed as constant, as will be discussed in section 4.5.4. Therefore, the short gate structure is expected to have the highest amplification of the four DEPFET designs.

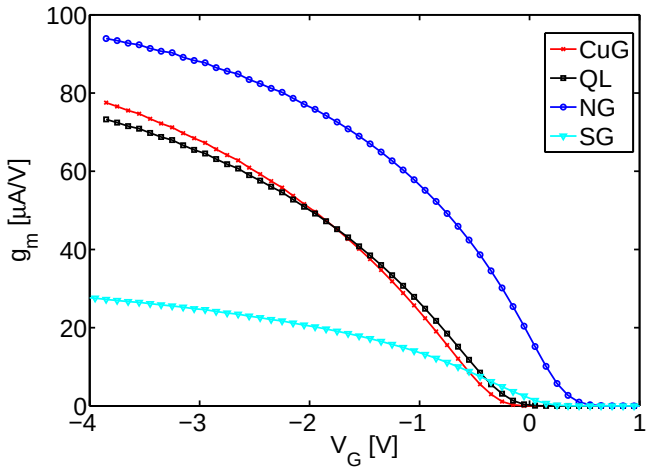
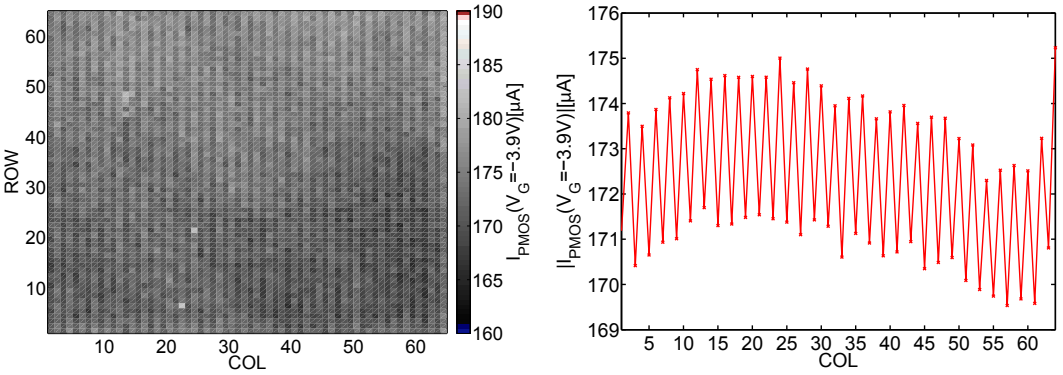


Figure 3.3.14.: PMOS transconductance g_m for the four representative pixel of the different DEPFET designs: QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate. g_m is the absolute slope of the transfer characteristics shown in figure 3.3.3.

The PMOS transconductance curves g_m (V_G) for the different DEPFET designs are depicted in figure 3.3.14. According to equation 2.2.20, the curves are expected to be linear but they are not. This is another evidence for the presence of short channel effects as well as three dimensional effects owing to the circular design. In [65] it has been reported on short channel effects for PMOS devices with a relation of gate length to gate oxide thickness $\frac{L}{d_{Ox}} = 66$ predicted by the constant field devices scaling rules [66]. For the IS devices the relation is $\frac{L}{d_{Ox}} \leq 28$. Hence, short channel effects like velocity saturation and g_m degradation are expected for the presented DEPFETs in addition to the charge sharing explained for the V_{Th} shift. For a detailed discussion of short channel effects see [29, 28].

Even-odd effect



(a) Pixel map of the transistor current in on-state for a cut gate (CuG) device.

(b) Average transistor current $|I_{\mathrm{PMOS}}|$ of all columns for a given gate voltage V_{G} = -3.9 V.

Figure 3.3.15.: Pixel of adjacent columns show an transistor current I_{PMOS} variation owing to the direct wafer lithography (DWL). The variation is also-called even-odd effect.

When the transistor current I_{PMOS} for a given gate voltage V_{G} = -3.9 V is plotted for every pixel of a matrix, the resulting image shows vertical stripes as displayed in figure 3.3.15a. The stripe feature can be seen even better by looking at the average transistor current I_{PMOS} per matrix column shown in figure 3.3.15b. A variation between adjacent columns can be seen clearly. The transistor current of even columns is higher than that of odd columns. This effect is called the even-odd effect.

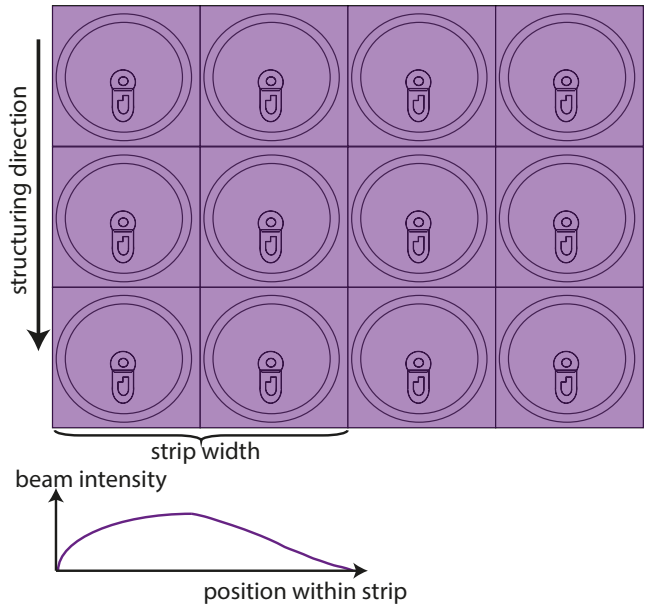


Figure 3.3.16.: Structuring of the photo resist using direct wafer lithography (DWL). The solid blue curve shows the distribution of the laser spot intensity [53].

It occurs due to systematic variations of the structure dimensions, which are caused by the Direct Wafer Lithography (DWL) as mentioned in [67]. Applying DWL, the photoresist is structured by scanning it in 200 µm wide strips in parallel to the pixel columns, as shown in figure 3.3.16. Neither the laser spot intensity is constant within one line nor is the line-to-line position. Hence, small length to width variations occur within one strip. The most sensitive part of the DEPFET for this kind of production variations is the gate length L. Variations in the gate are visible more clearly in the length than in the width because of its smaller total size. Due to the pixel width of 100 µm, two pixels are exposed simultaneously causing a periodical variation every second column. In order to make the effect comparable between devices, the percentage of the even-odd effect of the transistor current from column n to column n+1

$$EvenOdd[\%] = \frac{|I_{\mathrm{PMOSn}} - I_{\mathrm{PMOSn+1}}|}{0.5 \cdot (I_{\mathrm{PMOSn}} + I_{\mathrm{PMOSn+1}})} \cdot 100 \tag{3.3.1}$$

is introduced. The results for *EvenOdd* are shown in figure 3.3.17.

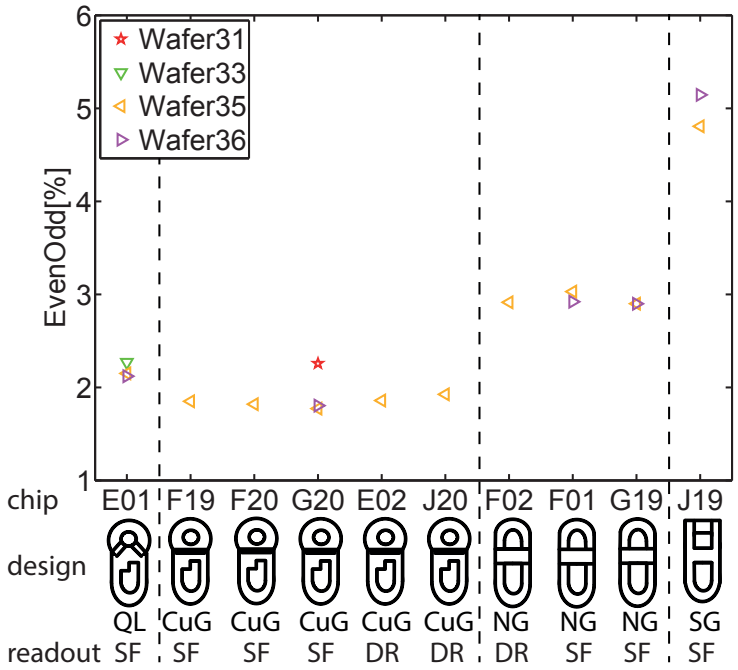


Figure 3.3.17.: Average percentage of the even-odd effect *EvenOdd* per die for all 17 pixel-wise characterized devices.

As expected, technology tolerances have a higher impact on the transistor behavior of the narrow gate and short gate design with their smaller gate dimensions than on cut gate and quasi linear design. These technology tolerances cause variations of the transistor current I_{PMOS} for a fixed gate voltage per die. In figure 3.3.17 no error bars representing the full width per die are shown because *EvenOdd* is already an averaged value. The gate length variation ΔL of adjacent pixel that causes the even-odd effect, can be determined by rearranging equation 2.2.18 to the gate length L. Note that this assumes ΔL to be the only feature change introduced. ΔL and *EvenOdd* summarized per design are presented in table 3.3.8.

	Cut Gate	Quasi Linear	Narrow Gate	Short Gate
EvenOdd [%]	1.9	2.2	2.9	5.0
ΔL [%]	1.5	1.5	2.1	3.9

Table 3.3.8.: Mean percentage of the even-odd effect determined at V_G =-3.9 V over all chips from every DEPFET design as well as the according gate length variation ΔL.

The achieved production homogeneity is illustrated by a gate length variation ΔL of less than 2.3 % for all designs despite of short gate with $\Delta L = 3.9$ %. It was already shown for MIXS macropixel matrices [9], that the ASTEROID readout ASIC can cope with the resulting deviation of V_G for a fixed transistor current I_{PMOS} during the detector operation in source follower configuration. Thus, the production homogeneity does not need an improvement in the scope of Athena. When the homogeneity should be increased anyhow, the lithography steps can be performed e.g. with electron beams or nanoimprinting instead of DWL.

3.3.3. Output characteristics

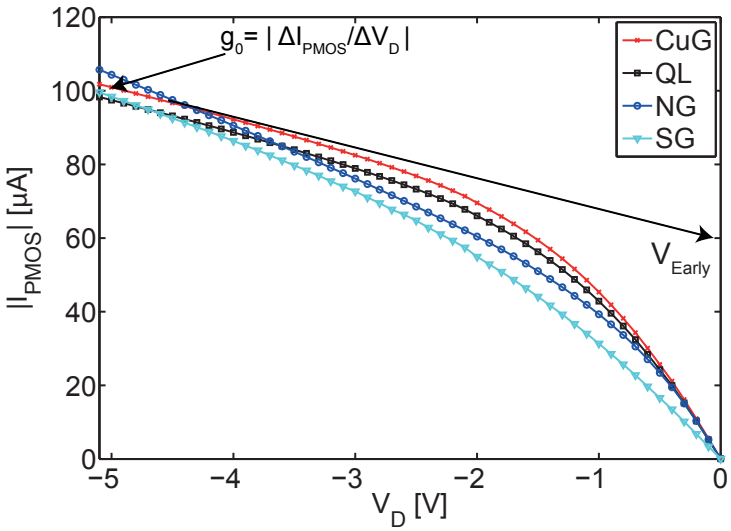


Figure 3.3.18.: The output characteristics of one representative pixel for each design from the same wafer: QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate. The parameter extraction points for the conductance g_0 and the inverse channel length modulation factor $\lambda = 1/V_{Early}$ are marked for the cut gate (CuG) curve.

A typical data set of the output characteristics for the four DEPFET variants is depicted in figure 3.3.18. The performance parameters extracted from the output characteristics of the DEPFET PMOS are the conductance g_0 and the inverse channel length modulation factor λ i.e. the Early voltage V_{Early}. These parameters provide information about the variation of the effective channel length of the PMOS in the saturation region and thus, about the stability of the DEPFET performance at its point of operation. The output characteristics have been measured only during the

pixel-wise characterization because the second Switch and SMU have not been available for the column-wise measurements. Hence, there are no column-wise parameters provided for this set of measurements.

Channel length modulation

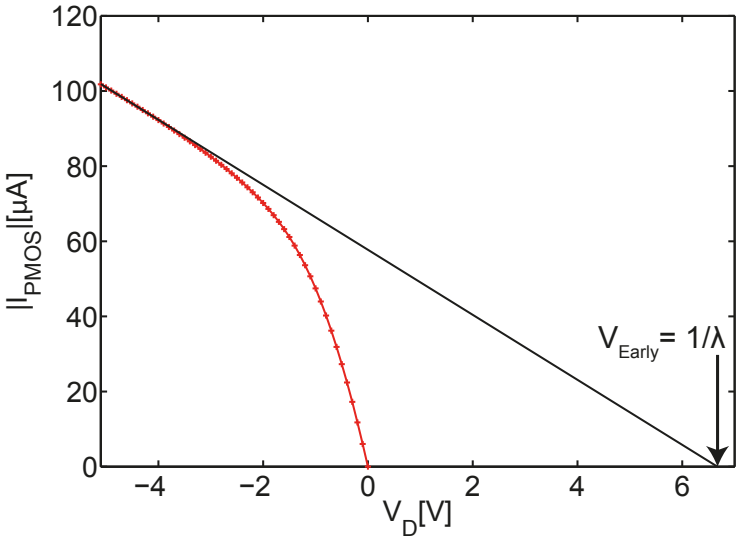


Figure 3.3.19.: The determination of the channel length modulation parameter $1/\lambda$ $=V_{\mathrm{Early}}$ for the cut gate (CuG) characteristics of a single pixel. The linear extrapolation is done using 10 measurement points between V_{D} = -5.1 V and V_{D} = -4.1 V.

As explained in section 2.2.2, the inversion layer shortens starting at the channel length L when V_{DS} is increased above $V_{\mathrm{DS,sat}}$. The reduction of the effective channel length is represented by the channel length modulation factor λ. The determination of λ from the output characteristics of a cut gate device is displayed in figure 3.3.19. The output characteristics is extrapolated linearly using 10 measurement points between V_{D} = -5.1 V and V_{D} = -4.1 V because there the curve has its most linear slope for all designs. The intersection of the extrapolation with the x-axis then gives V_{Early}, which is the reciprocal of the channel length modulation factor λ.

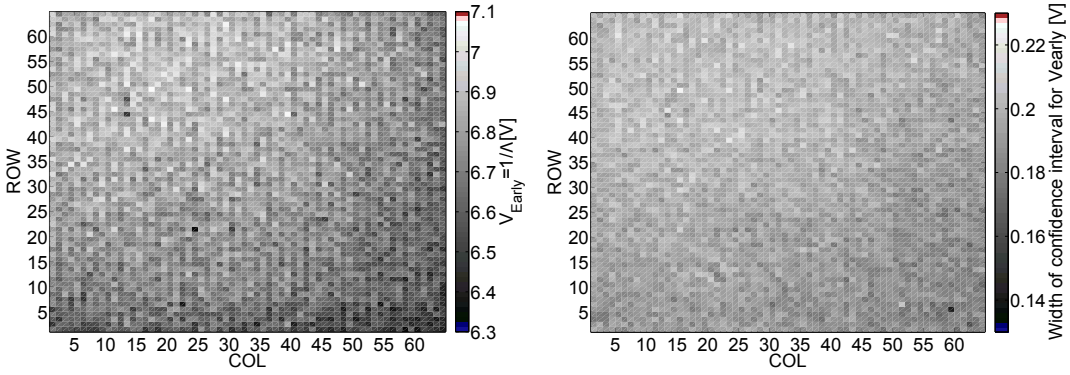
The extraction method for V_{Early} using an extrapolation implies a confidence interval. As extrapolation formula

$$I_{\mathrm{PMOS}} = m \cdot V_{\mathrm{D}} + n$$

is used with m as slope and n as intersection with the y-axis. V_{Early} is then calculated by

$$\frac{1}{\lambda} = V_{\mathrm{Early}} = \frac{0 - n}{m}$$

Both, n and m have a confidence interval from the fitting procedure. Thus, for V_{Early} the worst case confidence interval is determined. A pixel map of V_{Early} from a cut gate device is shown in figure 3.3.20a and the corresponding maximum width of the confidence interval in figure 3.3.20b. The maximum width is with 0.22 V negligible



(a) Pixel map of the Early voltage V_{Early}

(b) Pixel map of the maximum width of the confidence interval for V_{Early}

Figure 3.3.20.: Pixel maps from device F20 (cut gate) of wafer 35 show representative for all devices that the maximum width of the confidence interval for V_{Early} with 0.22 V is negligible compared to the deviation of V_{Early} over all pixels of one device with 0.8 V.

compared to the inter-pixel variation Δ_{Die} of 0.8 V for one cut gate device. Table 3.3.9 shows that the confidence interval of V_{Early} for the three other DEPFET designs is also small compared to the full width per die. Thus, instead of the confidence interval the full width per die is given in the following figures.

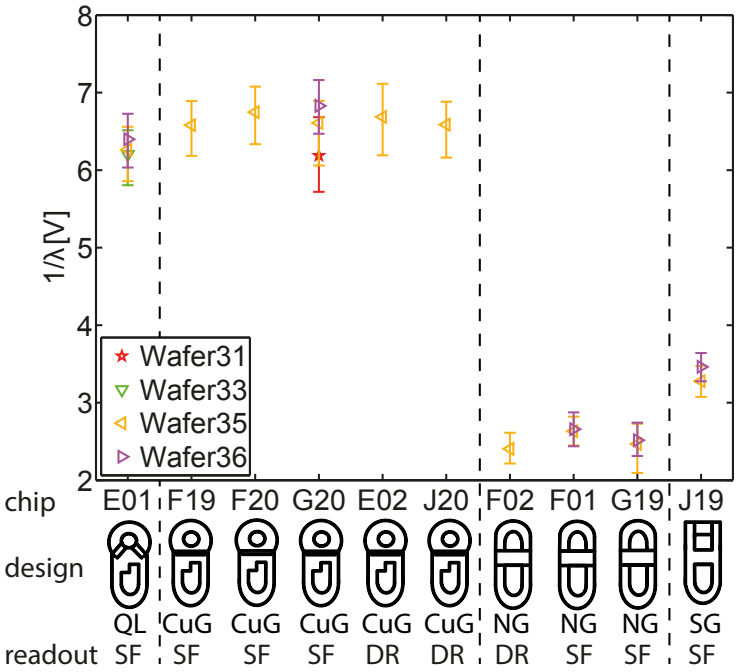


Figure 3.3.21.: Mean inverse channel length modulation $1/\lambda$ of the PMOS transistor for the pixel-wise characterized sample devices. The error bar represents the full parameter width per die.

The inverse channel length modulation is depicted in figure 3.3.21. The higher $1/\lambda$ the smaller is the pinch-off of the channel in the saturation region with more negative V_{D}. $1/\lambda$ is proportional to the channel length L of the transistor. That is why $1/\lambda$ of cut gate and quasi linear with $L = 4.9$ µm is greater than for narrow gate and short gate designs with $L = 2.9$ µm. The derived $1/\lambda$ are summarized for every design in table 3.3.9.

	Cut Gate	Quasi Linear	Narrow Gate	Short Gate
mean $1/\lambda$ $[V] = V_{\mathrm{Early}}$	+6.6	+6.3	+2.5	+3.4
maximum width of confidence interval $[V]$	0.21	0.20	0.06	0.14
mean Δ_{Die} $1/\lambda$ $[V]$	0.8	0.7	0.5	0.4

Table 3.3.9.: Mean over all chips from every DEPFET design according to the sample size in table 3.3.4. Mean Δ_{Die} is the average full width of the parameter per die.

The modulation of the channel length increases the detector gain g_{d} according to equation 2.2.34 because of

$$C_{\mathrm{G}} = C'_{\mathrm{G}} \cdot W \cdot L_{\mathrm{effective}} \text{ with } L_{\mathrm{effective}} < L$$

The increased gain might also lead to a better readout noise ENC_{Filter} but as the DEPFET has an outstanding noise in the source follower configuration already, the improvement is expected to be negligible. The difference of 0.9 V for V_{Early} between narrow gate and short gate indicates the presence of three-dimensional effects and it is supposed that for the small gate width $W = 7$ µm of the short gate also width modulation occurs. Width modulation could compensate a part of the channel length modulation and may balance the relation $\frac{W}{L}$. In view of the PMOS bias shift owing to radiation damages during the Athena mission, a design with small channel length modulation or so to say high $1/\lambda$ should be preferred e.g. the quasi linear design. For such a device, a stable detector performance for a wide range of transistor bias voltages is expected.

Output conductance

The output conductance g_0 is derived as the slope of the output characteristics at V_{D} = -5 V and $V_{On} = V_G(|I| = 100\ \mu A)$ as done before for the transconductance of the transfer characteristics in section 3.3.2. The derived g_0 for the pixel-wise measured output characteristics for all designs is depicted in figure 3.3.22.

The conductance g_0 of cut gate and quasi linear structures match because of their similar design. The higher g_0 for narrow gate and short gate devices are consistent with equation 2.2.21, according to which g_0 is proportional to $1/L$. The mean conductance g_0 for the four DEPFET designs is summarized per design in table 3.3.10. There is a difference of 1.7 $\frac{\mu\mathrm{A}}{\mathrm{V}}$ between the average conductance g_0 of the narrow gate and short gate design. It cannot be excluded, that in addition to the gate length modulation, a width variation occurs for the short gate devices as mentioned for the channel length modulation factor.

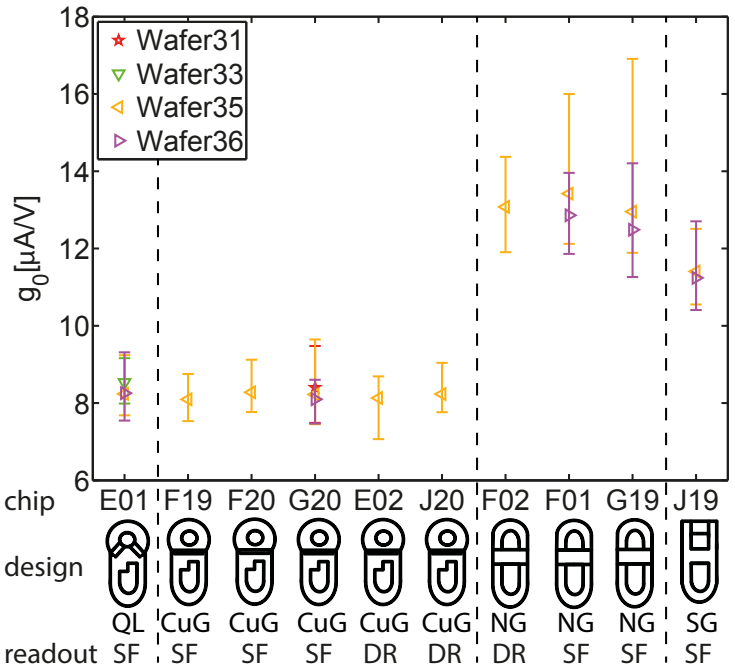


Figure 3.3.22.: Average output conductance g_0 for the defined on-state $V_{On} = V_G(|I| = 100\ \mu A)$ with V_D = -5 V of the PMOS transistor. The error bar marks the full width per die for the 17 pixel-wise characterized IS devices.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}
g_0 $[\mu A/V]$	8.2	1.5	8.3	1.5	13.0	3.3	11.3	2.1

Table 3.3.10.: Mean conductance g_0 over all pixel-wise characterized dies from every DEPFET design. Mean Δ_{Die} is the average full width of the parameter per die.

A closer look at the output conductance curves g_0 (V_D) in figure 3.3.23 indicates the presence of three dimensional effects and short channel effects as mentioned for g_m and as explained for V_{Th}. According to equation 2.2.21, g_0 (V_D) is expected to be constant for an ideal PMOS transistor with long and wide linear conduction channel but in the figure it is obviously not for all four design variants. In addition to the non-linearity, the short gate design shows in g_0 (V_D) several erratic areas. The effect was examined and the irregular curve shape has been found at the same voltages for all pixels of the measured short gate dies from all wafers but no pattern has been recognized. Nevertheless, the erratic behavior is an indicator for instability of the short gate device in the drain voltage region below the saturation voltage. Apart from the fact, that the DEPFET is operation in saturation, instabilities are unwanted and should be examined closer in the future with three-dimensional simulations.

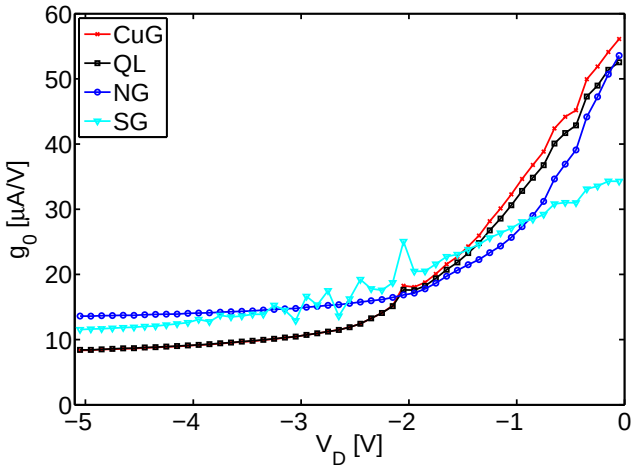


Figure 3.3.23.: PMOS output conductance curves g_0 for the different DEPFET designs: QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate. It represents the slope of the curves shown in figure 3.3.18.

Difference theoretical MOSFET to DEPFET

In order to support the estimation of the presence of short channel effects in the DEPFET designs, the output characteristics is fitted using equations 2.2.17

$$I_{\mathrm{PMOS}} = -\frac{W}{L} \cdot \mu_{\mathrm{P}} \cdot C'_{\mathrm{G}} \left(V_{\mathrm{GS}} - V_{\mathrm{Th}} - \frac{V_{\mathrm{DS}}}{2} \right) \cdot V_{\mathrm{DS}}$$

in the linear region and 2.2.18

$$I_{\mathrm{PMOS}} = -\frac{W}{2L} \cdot \mu_{\mathrm{P}} \cdot C'_{\mathrm{G}} \left(V_{\mathrm{GS}} - V_{\mathrm{Th}} \right)^2 \cdot \left(1 - \lambda V_{\mathrm{DS}} \right)$$

in the saturation region from section 2.2.2. The internal gate is empty, hence no influence from it is expected. V_{GS}, V_{Th}, V_{DS} and λ are taken from the measurement data. The free fitting parameter is β that is defined according to equation 2.2.19 as

$$\beta = \frac{W}{L} \cdot \mu_{\mathrm{P}} \cdot C'_{\mathrm{G}}$$

The fitting parameter will be compared to the theoretical value of β, which is calculated using $C'_{\mathrm{G}} = 1.76 \pm 0.03 \cdot 10^{-4}\ \frac{\mathrm{F}}{\mathrm{m}^2}$ determined with equation 2.2.4. For the calculation of the theoretical β, the hole velocity μ_{P} is required. Thus, μ_{P} was derived from the transfer characteristics in the linear region of a test structure from an earlier DEPFET production using the same gate insulator stack but with a gate width $W = 120$ µm and a length $L = 60$ µm instead. For these gate dimensions, the absence of short channel effects is assumed. The measurement data and the fit are shown in figure 3.3.24. The determined hole velocity μ_{P} is $0.0214 \pm 0.0001\ \frac{\mathrm{m}^2}{\mathrm{Vs}}$, which is low compared to the expected $0.03\ \frac{\mathrm{m}^2}{\mathrm{Vs}}$ given in [68]. Possible reasons for that are a higher doping rate as foreseen in the transistor channel or a high density

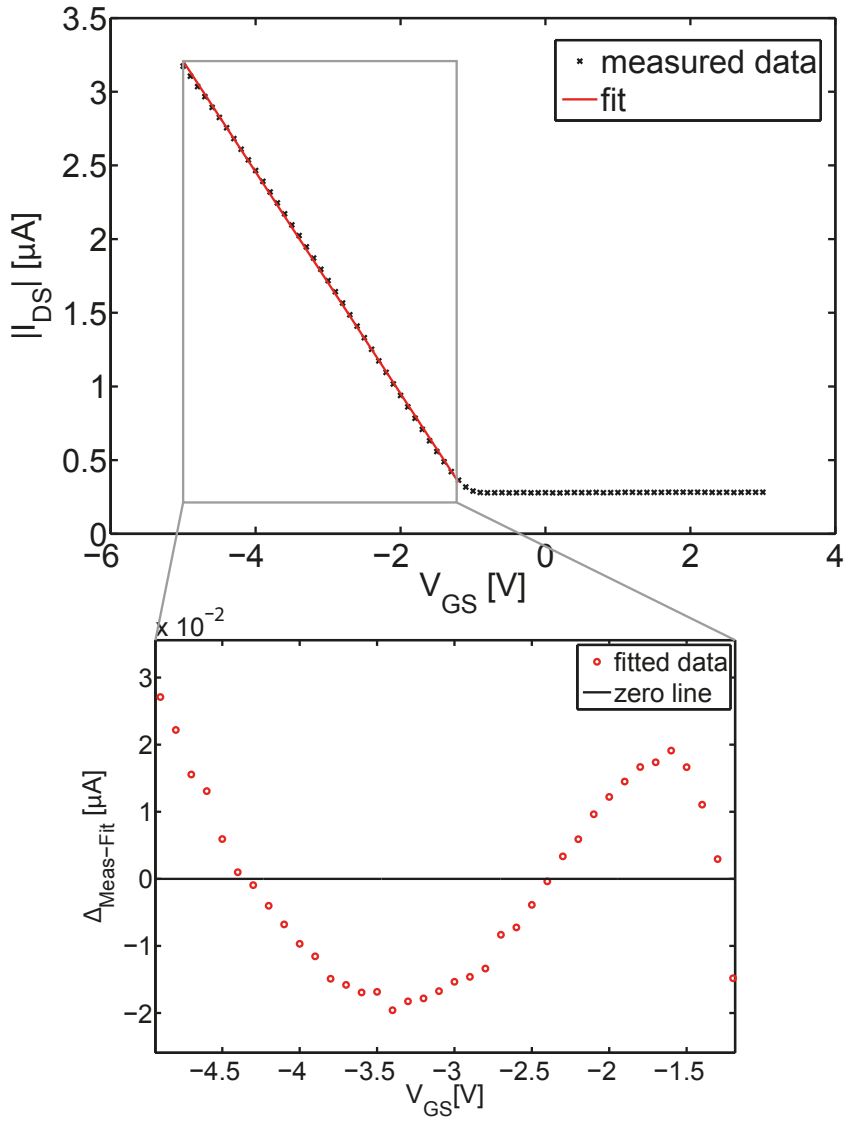


Figure 3.3.24.: Ohmic transfer characteristics of a PMOS test structure with no estimated short channel effects. The hole velocity μ_P is derived as $0.0214 \pm 0.0001 \frac{m^2}{Vs}$ using a fit after equation 2.2.17 (I_{PMOS} (V_{DS}) for the linear region). The inset shows the difference between measured data point and the fitting results. The relative difference is less than 2%.

of surface traps.

Here, the fitting of the output characteristics is shown for the short gate design (single pixel of die J19 from wafer 35), which is the only structure with a linear transistor gate. For completeness the results of the fits from the other designs are presented in the appendix in section A.1.4. The output characteristics of the short gate design and its fit in the linear and saturation region are depicted in figure 3.3.25. As mentioned before the free fitting parameter is β. For the fixed parameters measurement values for that exact pixel are used. The applied gate-source potential used for the

I_{PMOS} (V_{DS}) measurement is V_{GS} = -4.84 V. From the transfer characteristics a threshold voltage of V_{Th} = +0.17 V was derived for the device. The channel length modulation in the saturation region is determined to be $1/\lambda$ = 3.27±0.14 V.

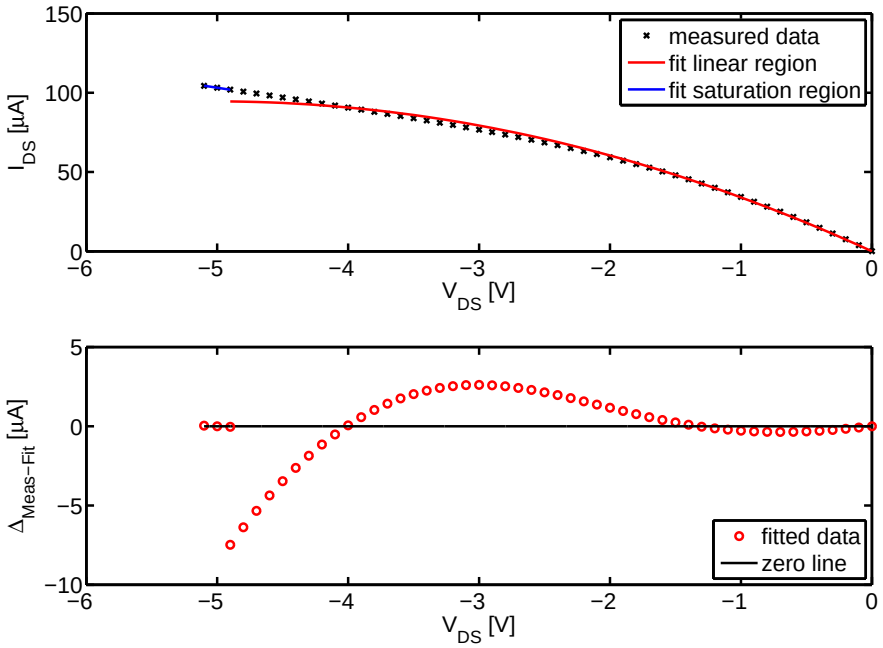


Figure 3.3.25.: Output characteristics of short gate (SG) single pixel with fits in the linear region (red) and in saturation (blue) with β as free parameter and given V_{GS} = -4.84 V, V_{Th} = +0.17 V, $V_{\mathrm{DS,sat}}$ = -5.1 V and $1/\lambda$ = 3.27±0.14 V. The bottom graph shows the difference between measured data point and fitting result.

The difference between the theoretical PMOS curves and the measurement data are obvious. In addition, the free fit parameter β differs with $\beta_{fit,lin} = 7.5 \pm 0.06 \ \frac{\mu A}{V^2}$ and $\beta_{fit,sat} = 3.3 \pm 0.01 \ \frac{\mu A}{V^2}$ for both regions. When the gate width of the short gate design W = 7 µm and the length L = 2.9±0.06 µm including the error due to the even-odd effect as well as μ_{P} and C'_{G} are inserted in equation 2.2.19, the theoretical β is

$$\beta_{SG,theo} = \frac{7 \ \mu m}{2.9 \pm 0.06 \ \mu m} \cdot 0.0214 \pm 0.0001 \ \frac{m^2}{Vs} \cdot 1.76 \pm 0.03 \cdot 10^{-4} \ \frac{F}{m^2} = 9.1 \pm 0.35 \ \frac{\mu A}{V^2} \tag{3.3.2}$$

Compared to the theoretical $\beta_{SG,theo}$ both fits give smaller values. This attributes to short channel effects. Such effects can be charge sharing of the transistor channel with the p-contacts, which has been explained earlier, leading to the degradation of μ_{P} and the threshold voltage shift. It is also likely that the adjacent clear structure has influence on the behavior of the PMOS transistor. For a detailed investigation of this topic linear test structures with varying gate width and length as well as with and without adjacent clear structure need to be fabricated and studied. The

presence of short channel effects do not hamper the functionality of the DEPFET but embarrass the undisputed assignment from measured effects to physical effects. Hence, the comparison of the four DEPFET designs can be done only in a qualitative manner and not quantitatively.

3.3.4. Clear characteristics

As explained in section 2.2.3, the clear structure is needed to empty the internal gate during readout. For which clear and clear gate voltages the electrons collected in the internal gate are fully removed, is investigated by measuring the DEPFET specific clear and clear gate characteristics.

Onset of the clear

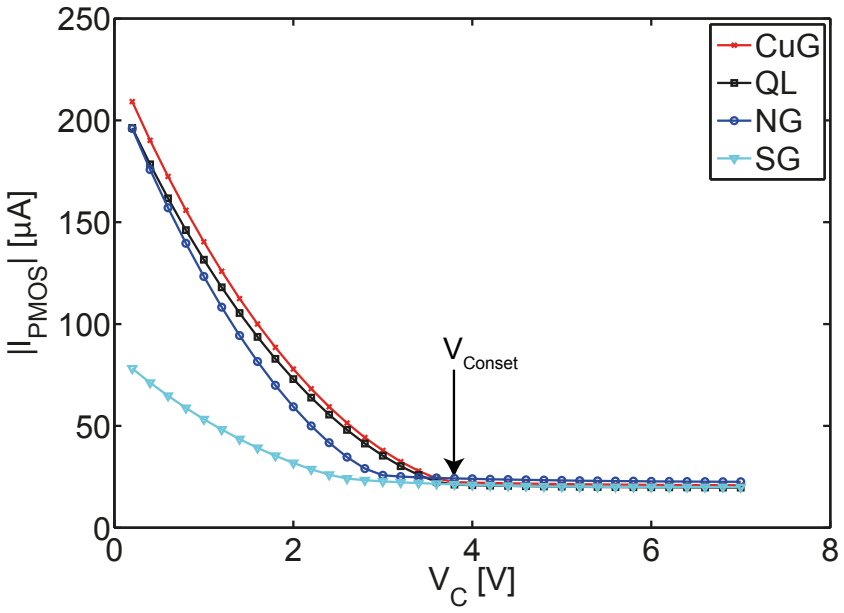


Figure 3.3.26.: The clear characteristics of one typical pixel for each design from the same wafer: QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate. The extracted onset of the clear V_{Conset} is marked for the cut gate (CuG) characteristics.

A typical data set for $I_{PMOS}(V_C)$ for all four designs with the extraction point for the onset of the clear V_{Conset} is depicted in figure 3.3.26. The clear gate is set open with +5 V. Thus, there is no potential barrier between internal gate and clear contact. The gate is also opened with a sufficiently negative bias to allow a constant transistor current $|I_{\mathrm{PMOS}}| = 20\ \mu\mathrm{A}$. The clear potential V_{C} is decreased until I_{PMOS} increases. When the clear voltage V_{C} becomes too low, the PMOS current I_{PMOS} rises because of electrons accumulating in the potential minimum. As mentioned in section 3.2, the electrical qualification is done at room temperature. Hence, there is thermal generation in the silicon bulk. In addition, charge can be injected from the clear contact into the internal gate. When the clear contact is biased sufficiently positive,

this leakage current is drained and no charge injection is possible. If not, the transistor current will increase, as shown in figure 3.3.26, due to mirror charges induced in the channel by electrons collected in the internal gate as described in section 2.2.3.

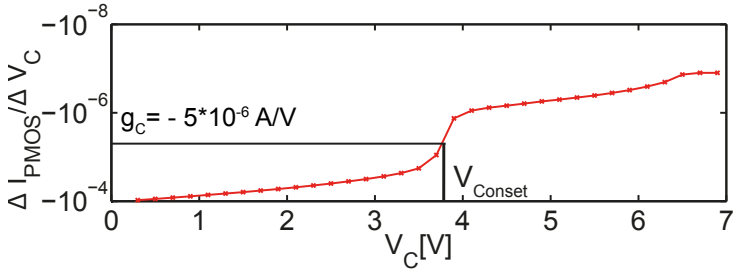


Figure 3.3.27.: Slope of the clear characteristics for the cut gate (CuG) design from figure 3.3.26. The onset of the complete clear V_{Conset} is defined at a slope of $g_C = -5 \cdot 10^{-6}$ $\frac{\mathrm{A}}{\mathrm{V}}$.

It can be seen, that I_{PMOS} increases rapidly for clear voltages less than about 4 V. To gain a parameter that can be compared for all devices, V_{Conset} defined as the clear voltage for the onset of the complete clear, is introduced. It is determined from the first derivative of the measurement curve, shown in figure 3.3.27. V_{Conset} is defined at a slope of $g_C = 5 \cdot 10^{-6}$ $\frac{\mathrm{A}}{\mathrm{V}}$ representing a PMOS current change ΔI_{PMOS} of 5 % per measurement step $\Delta V_{\mathrm{C}} = 0.2$ V.

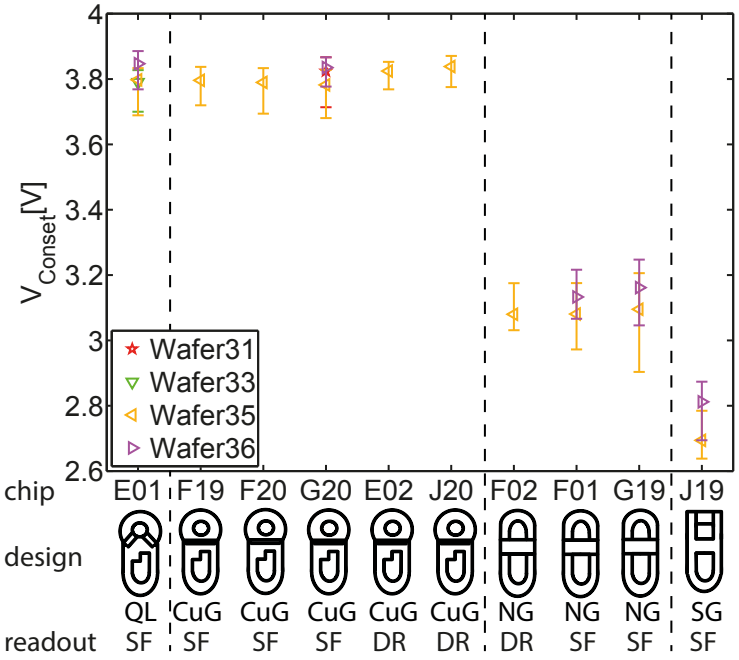


Figure 3.3.28.: Average onset voltage of the clear V_{Conset} for all pixel-wise characterized devices. The full width per die is shown as error bar for every device.

In figure 3.3.28 the onset of the clear V_{Conset} is displayed for the pixel-wise characterized devices. As seen for all extracted parameters of the transfer and output characteristics before, the devices group within design. It is possible to see the clear process as a two step process, where the electrons drift first under the opened clear gate and then drift into the clear contact. For the narrow gate and short gate devices, a lower V_{C} is needed to start the complete clear compared to the other structures. This is due to a linearly directed electric field between internal gate and clear contact. When the clear gate is opened, the electrons, which are collected in the internal gate, are attracted earlier by the clear potential. The results of the column-wise measured clear characteristics are discussed in the appendix A.1.5.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}
V_{Conset} $[V]$	+3.81	0.12	+3.81	0.13	+3.11	0.20	+2.75	0.16

Table 3.3.11.: For all designs V_{Conset} of the pixel characterized devices is summarized according to table 3.3.4. The deviation within the design groups is given as the average full width Δ_{Die}.

In table 3.3.11 the mean of V_{Conset} over all devices per design is shown. V_{Conset} groups within a range of 1.1 V for all devices. The average full width of V_{Conset} per die differs for the designs apparently with the gate dimensions as seen for the parameters from the transfer or output characteristics. This indicates that the etching variations for polysilicon owing to DWL also affects the clear structure.

In figure 3.3.29 the maps of the onset voltage of the clear V_{Conset} for several devices with respect to their position on the wafer are shown. Because of the different DEPFET layouts, V_{Conset} is normalized to its minimum value for every die. A concentric structure is visible for all devices with varying markedness for the different DEPFET designs. It is supposed that this structure is a result of the resistivity variation of the high ohmic (3500 - 7000 Ωcm) float zone silicon wafer material [9] with a diameter of 150 mm. It has been reported from silicon manufacturers, that these structures form during the production of the single crystal ingot [53]. The influence of any implantation can be precluded as the used implantation system cannot form circular structures with respect to the wafer center.

Onset of the clear gate

Another part of the clear characteristics is the determination of the onset of the complete clear at clear on potential of $V_{\mathrm{C}} = +10$ V while decreasing the clear gate voltage V_{CG}. Hence, it is tested, when the clear potential of $V_{\mathrm{C}} = +10$ V is separated from the internal gate, so that electrons are collected there and influence the transistor current I_{PMOS}. To do so, gate and clear gate are opened and allow a transistor current $|I_{\mathrm{PMOS}}| = 50$ µA. Then the clear gate potential V_{CG} is decreased until the transistor current increases. A typical set of measurement curves is shown in figure 3.3.30.

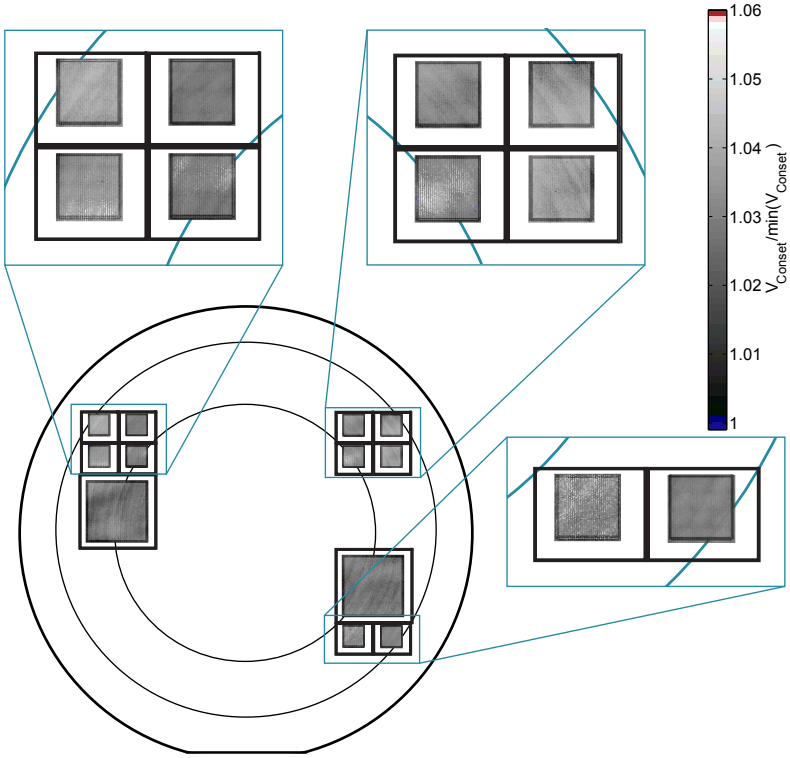


Figure 3.3.29.: Maps of the onset voltage of the clear V_{Conset} for two MIXS macropixel matrices and the surrounding 10 IS prototypes with respect to their position on the wafer 35. V_{Conset} is normalized to the minimum value for every die. A concentric structure is visible due to the resistivity variation of the high ohmic float zone silicon wafer material [9].

Here, the onset of the complete clear is defined for a clear gate potential called V_{CGonset}, that is calculated in the same way as V_{Conset} (see the previous section) at a slope of $g_{CG} = -5 \cdot 10^{-6}\ \frac{\mathrm{A}}{\mathrm{V}}$ as displayed in figure 3.3.31.

In figure 3.3.32 the distribution of V_{CGonset} over a cut gate device is shown. As seen before on V_{Conset} in figure 3.3.29, a ring structure is visible due to the variation of the wafer materials resistivity. The bulk resistivity is decisive for how high the potential drop between the internal gate and the clear contact needs to be, in order to attract the signal electrons stored in the internal gate.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}
$V_{CGonset}$ $[V]$	-0.92	0.72	+0.02	0.68	-0.68	0.36	-0.19	0.55

Table 3.3.12.: Mean clear gate onset voltages V_{CGonset} determined for the clear gate characteristics over all single pixel characterized chips from every DEPFET design. Mean Δ_{Die} is the average full width of the parameter per die.

The mean V_{CGonset} per die is shown in figure 3.3.33. It can be seen that cut gate

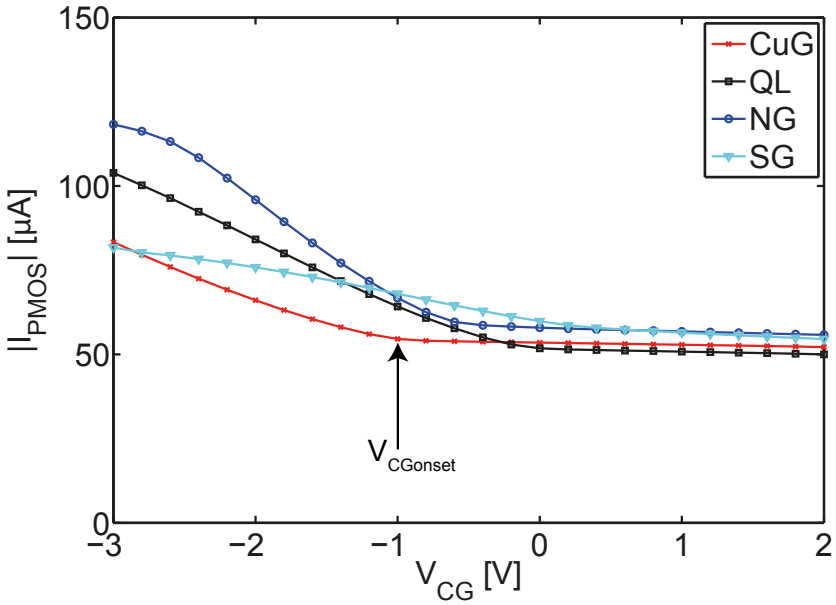


Figure 3.3.30.: The clear gate characteristics of one representative pixel for each design from the same wafer: QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate. The marked V_{CGonset} extraction point belongs to the cut gate (CuG) curve.

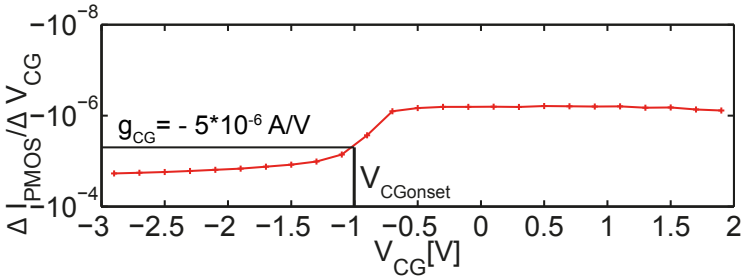


Figure 3.3.31.: Slope of the clear gate characteristics for the cut gate (CuG) design from figure 3.3.30. The onset of the complete clear V_{CGonset} is defined at a slope of $g_{CG} = -5 \cdot 10^{-6} \ \frac{\mathrm{A}}{\mathrm{V}}$.

and narrow gate structures have V_{CGonset} of about -0.92 V and -0.68 V respectively. For the quasi linear design the potential barrier between clear and internal gate is much lower than for all other device, as evidenced by a positive V_{CGonset}. The short gate structure shows a more positive V_{CGonset}, too. The measured devices from wafer 36 have more negative V_{CGonset} values than those of wafer 35. Wafer 36 has been produced using a polysilicon 1 or clear gate thickness of 500 nm instead of 600 nm. According to equation 2.2.2, the MOS capacitance is inverse proportional to its thickness. Hence, the V_{CGonset} must change because the amount of charge carrier that need to be transferred to the clear contact is constant. The mean values of V_{CGonset} for all four designs are summarized in table 3.3.12. The clear gate voltage for the onset of the complete clear for the column-wise measurements $V_{\mathrm{CGonset64}}$ is presented in the appendix A.1.6.

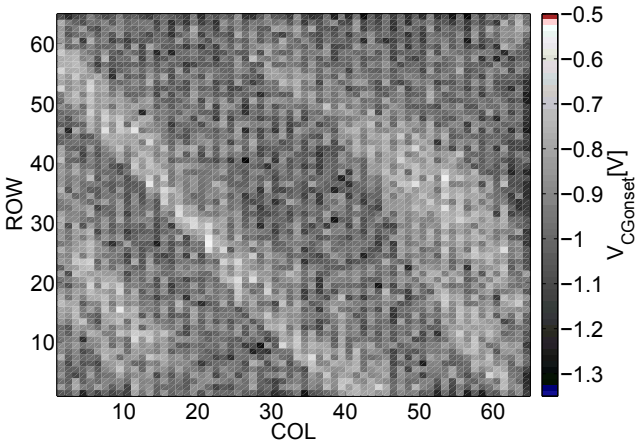


Figure 3.3.32.: Pixel map of the onset of the clear gate V_{CGonset} for the cut gate (CuG) chip F20 of wafer 35. As shown for V_{Conset}, the concentric structure due to the bulk resistivity variation is visible here, too.

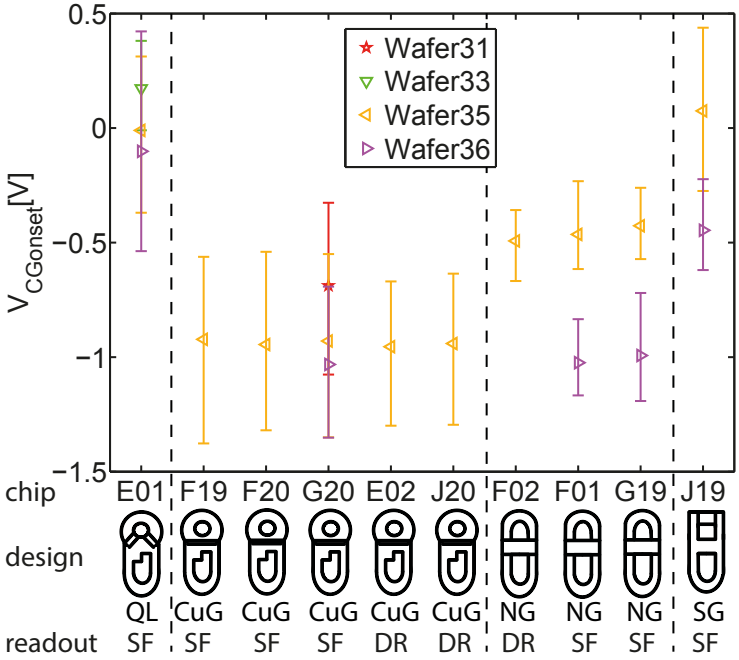


Figure 3.3.33.: Mean of V_{CGonset} for all 17 pixel-wise characterized devices. The plotted error bar represents the full width of V_{CGonset} for every device.

3.4. Summary of the electrical qualification measurements

In preparation for Athena, the ideal DEPFET X-ray detector should fulfill four criteria as identified in the introduction in chapter 1:

1. The devices must be manufacturable in wafer-scale dimensions in order to meet the needed angular resolution and field of view. In addition to a high device yield, the homogeneity among the pixels of one wafer-scale chip must be manageable for the steering and readout ASICs.

2. The detector needs a high internal amplification, low noise and low leakage current as high spectral resolution and high detection sensitivity are required.

3. The detector must be addressable pixel-wise and the readout has to be fast to reach the required information throughput.

4. Space is a harsh environment. Thus, the detector must be radiation tolerant and needs a large window of operational voltages with stable detection performance.

The electrical qualification measurements give information about the yield and homogeneity and make predictions for internal amplification, noise and operational voltages. The remaining criteria are addressed by the spectroscopic measurements in the following chapter.

All in all the estimated yield learning is given by the electrical tests of the IS devices. The production reached a high yield for the IS structures with 70 defect free devices out of 80, which equals one defect in 10 cm^2 chip area. Nevertheless, the yield must be improved to less than one defect per 54 cm^2 in order to get the wafer-scale devices for Athena. Therefore, short-circuits within the polysilicon layers and between the aluminium layers must be prevented. Thus, the short gate layout has to be relaxed either by reducing the polysilicon 1 structure height or by increasing the channel length. For all designs despite the short gate, an increase of the isolator about 30 nm is helpful in order to increases the breakdown voltage between the polysilicon layers. Using a thicker nitride layer between the polysilicon structures is known to decrease the radiation hardness of the DEPFET [54] and it must be simulated whether this preventive action is applicable for Athena. In addition, an improvement of the inter-metal-isolator is suggested as well as one defreckle etching step after every aluminium deposition step because of the one percent silicon in the used sputter target. Another method used for the enhancement of the DEPFET production technology is the application of the hot de-ionized water treatment during the aluminium layer processing to reduce short circuits as a result of hillock formation.

As shown in section 3.3.2, the gate length variation ΔL resulting from the usage of DWL is less than 2.3% for all designs other than the short gate design, which shows 3.9%. That shows a great homogeneity over all devices and wafers. The ASTEROID readout ASIC can cope with the resulting deviation of V_G for a fixed transistor current I_{PMOS} during the detector operation in source follower configuration as shown

for MIXS. Thus, the production homogeneity does not need improvement in the scope of Athena. If the homogeneity shall be increased anyhow, the lithography steps can be performed e.g. with electron beams or nanoimprinting instead of DWL.

For all extracted parameters of the transfer, output and clear characteristics such as V_{Th}, V_{On}, g_{m}, *EvenOdd*, g_0, λ, V_{Conset}, V_{CGonset} the devices group with their design. This allows to clearly see differences in the operational parameters needed for different designs. The standard deviations within the devices itself and within the wafers are greater for the design variants with smaller gate dimensions, which can be explained again with DWL. Furthermore, no systematic differences can be seen between the wafers or the two production batches, despite of g_{m} variations for wafers 30 and 31 as explained through the thicker nitride layer in section 3.3.2. Additionally, V_{CGonset} differs between wafers manufactured with a clear gate thickness of 500 nm and 600 nm, which is caused by a change in the MOS capacitance. The used wafer material is also clearly reflected in the electrical qualification results of the onset of the clear in figure 3.3.29.

The distribution of the parameter within the designs follows in tendency the theoretical equations from section 2.2.2 but not exactly as seen in sections 3.3.2 and 3.3.3 for V_{Th}, g_{m}, g_0 and I_{PMOS} (V_{G}) curve shapes. This is evidence for the presence of short channel effects as well as three-dimensional effects that can e.g. be seen in the effects of interchanged source and drain potential as discussed in section 3.3.2. Owing to its complex three-dimensional structure, the DEPFET cannot be mapped with neither the ideal transistor equations nor existing models for short channel transistors as even for linear transistor geometries numerical calculations are not exact and very specific [38, 64]. For a detailed investigation of this topic, linear test structures with varying gate width and length as well as with and without adjacent clear structure need to be fabricated and studied. The presence of short channel effects does not hamper the functionality of the DEPFET but make the clear assignment of measured effects to physical effects difficult if not impossible. Hence, the comparison of the four DEPFET designs can be done only in a qualitative manner and not quantitatively.

So far the short gate design seems promising because of its low g_{m} that should result in a high DEPFET gain at low noise. But the electrical characterization is not sufficient for a final success evaluation because it cannot determine the dynamic properties of the pixels and their interaction, which will be discussed in the next chapter. To sum it up, at this point of the electrical testing all defect free matrices are well suited for the assembly of a detector system.

3.5. Definition of a concise electrical test

It was shown that by using the automated probe head, fine structures and technology influenced effects can be revealed, which cannot be seen with the much faster column-wise measurements. The results of column and pixel-wise measurements are comparable, as shown in section 3.3.2 and A.1.3 but they are not identical as the

column-wise measurement gives the average result for 64 transistors. Hence, depending on the required degree of detail and the available measurement time, the appropriate measurement set can be chosen.

Before building a detector system, the DEPFET matrix should be checked for short-circuits because the integration of a full detector with DEPFET matrix and ASICs is time consuming and expensive. The short-circuit test takes 32 s for 64 × 64 pixel resulting in 37 min for the 70 times larger 448 × 640 wafer-scale device for Athena.

For estimating operational parameters and testing for outliers, it is sufficient to do a more time-efficient measurement procedure without automated probe head. It was found that dominant outliers show up even for the measurement of 64 transistors in parallel. Increasing the number of transistors measured in parallel may decrease the sensitivity. Hence, the layout and fanout of the wafer-scale devices and the used needle card must be adapted accordingly. As will be described later in section 4.5.3, the operation window of clear V_{C} and clear gate voltages V_{CG} must be established using an oscilloscope in advance of spectroscopic measurements. Thus, for a concise test the measurement of the clear and clear gate characteristics can be shortened by increasing the step width to 0.5 V. Choosing either the I_{PMOS} (V_{G}) or I_{PMOS} (V_{D}) characteristics limits the testing time to about 656 s per 64 × 64 pixel leading to 816 h per full-size Athena die. For the pixel-wise characterization a total measurement time of 830 h has been accumulated and the measurement setup worked reliable during this period. Nevertheless, an additional parallelization for several 64 × 64 pixel boxes is necessary. Furthermore extra tests concerning switching time and potential drops should be established for the wafer-scale devices.

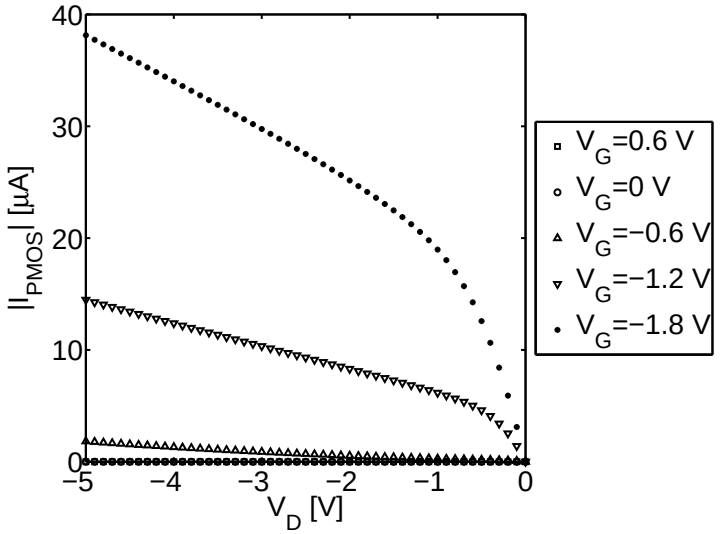


Figure 3.5.1.: Array of output characteristics for the cut gate (CuG) device F20 of wafer 35 measured for column 10 of row 1.

Nevertheless, to investigate the homogeneity and study details of the layout for flight devices, the pixel-wise test at least of the PMOS transistor is essential in order to reveal the number and exact position of outlier pixels. For further investigations of design variants, the full measurement procedure including transfer, output and clear characteristics should be measured.

The obtained measurement data can also be used in look-up-table systems such as Cadence Virtuoso Spectre Circuit Simulator. A thinkable application would be the simulation of the contribution on noise and achievable readout speed of the device itself in the detector system. Therefore, additional measurements of I_{PMOS} (V_{D}) arrays as shown in figure 3.5.1 are suggested, which even can replace I_{PMOS} (V_{G}).

4. Characterization of the spectroscopic performance

After the electrical qualification of the DEPFET designs, they need to be tested for their spectroscopic performance. The measurement setup, routines and data analysis tools used for the spectroscopic measurements as well as the results obtained are discussed in the following sections.

4.1. Scope of the spectroscopic measurements

According to the results from the quasi-static electrical characterization, all four DEPFET designs are suited for the integration of a full detector system. The purpose of the spectroscopic measurements is to test the dynamic behavior of the designs as well as their spectroscopic performance. With a measurement setup composed of newly designed printed circuit boards, which are described in section 4.2, and well known customized detection and analysis software, see section 4.4, the DEPFET detectors can be tested under stable and reproducible conditions that presented in section 4.3.

The spectroscopic measurements reveal how the transistor behavior translates into the detector performance. With these tests three out of the four criteria for Athena are addressed:

1. In sections 4.5.1 and 4.5.2, the influence of the leakage current, the detector amplification and the noise on the spectral resolution can be seen.

2. In section 4.5.3 it is investigated how stable the spectroscopic performance is under variation of the detector biasing. In later operation, this information can be used to e.g. compensate radiation damage [69] or sourcing tolerances of power supplies. For every bias voltage a large and stable operation window is desirable.

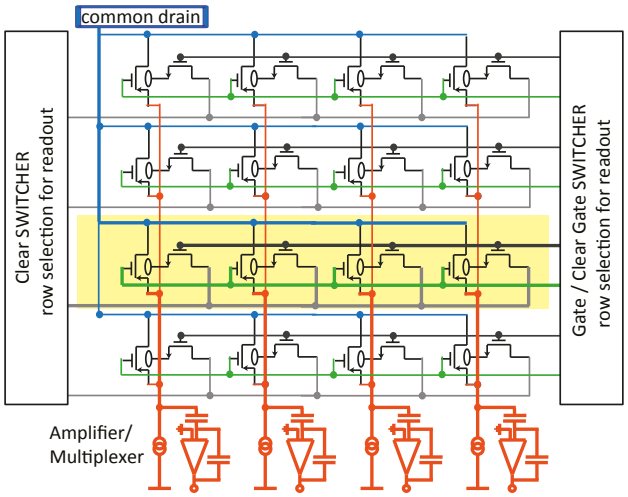
3. The readout speed limits are tested by varying the operation timing. The results obtained are also presented in section 4.5.3.

4.2. Detector setup

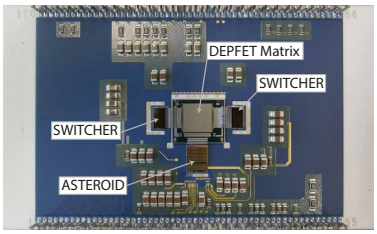
From every design type one source follower device was integrated into a full detector system. As all IS chips of wafer 35 are defect free, the following chips were selected as representative devices for the respective designs: F20 (cut gate), E01 (quasi linear), F01 (narrow gate) and J19 (short gate) (see tables 2.3.2 and 3.3.1). E01 and J19 are chosen because for those designs only one chip per wafer has been fabricated and

F20 as well as F01 are randomly picked as no significant difference between the cut gate (F19, F20, G20) and narrow gate devices (F01, G19) of wafer 35 was found.

4.2.1. Detector hybrid



(a) Connection principle for a 4 × 4 DEPFET matrix in source follower mode (adapted from [49]). The yellow box marks the selected row.



(b) Ceramic board with mounted DEPFET matrix, readout and control ASICs.

Figure 4.2.1.: DEPFET matrix for source follower readout: all drain contacts are biased as grid, the sources are connected column-wise to the amplifier / multiplexer ASIC (ASTEROID). Gates, clears and clear gates are connected row-wise and are controlled by SWITCHER ASICs.

As explained in section 2.2.4, pixel arrays with various sizes can be designed by combining DEPFETs as shown in figure 4.2.1a exemplarily for a 4 × 4 matrix. The drain contacts of the source follower matrices are biased globally for the whole matrix, whereas clear, clear gate and gate contacts are connected row-wise. Their potentials are switched via so-called SWITCHER ASICs [70]. The source contacts are connected column-wise and are read out in parallel with the ASTEROID as depicted in section 2.2.5.

For the operation of the source follower system shown in figure 4.2.1a, the drain is set to -5 V globally for the whole matrix. The gate of the row marked yellow in figure 4.2.1a is activated by the gate SWITCHER meaning its potential is set to V_{Gon} while all other gates remain in off-state at V_{Goff}. The transistor current $|I_{\mathrm{PMOS}}|$ is set to 100 µA by the current source of the ASTEROID. Then the source potential with the DEPFET's internal gate filled with signal electrons is recorded in parallel by the ASTEROID ASIC for the yellow marked row. Afterwards the clear potential for the selected row is switched from off to on-state by the clear SWITCHER and the clear gate by the gate SWITCHER. As described in section 2.2.5, if sufficient clear and clear gate voltages are applied, a conductive connection between clear and internal gate is established. All signal electrons from the internal gate are removed through the clear contact. Then the clear structure is deactivated and the ASTEROID ASIC

records the source potential again and builds the difference of the two records as output value. At last the gate for the row is turned off and the SWITCHER ASICs selects the next row.

4.2.2. Setup periphery

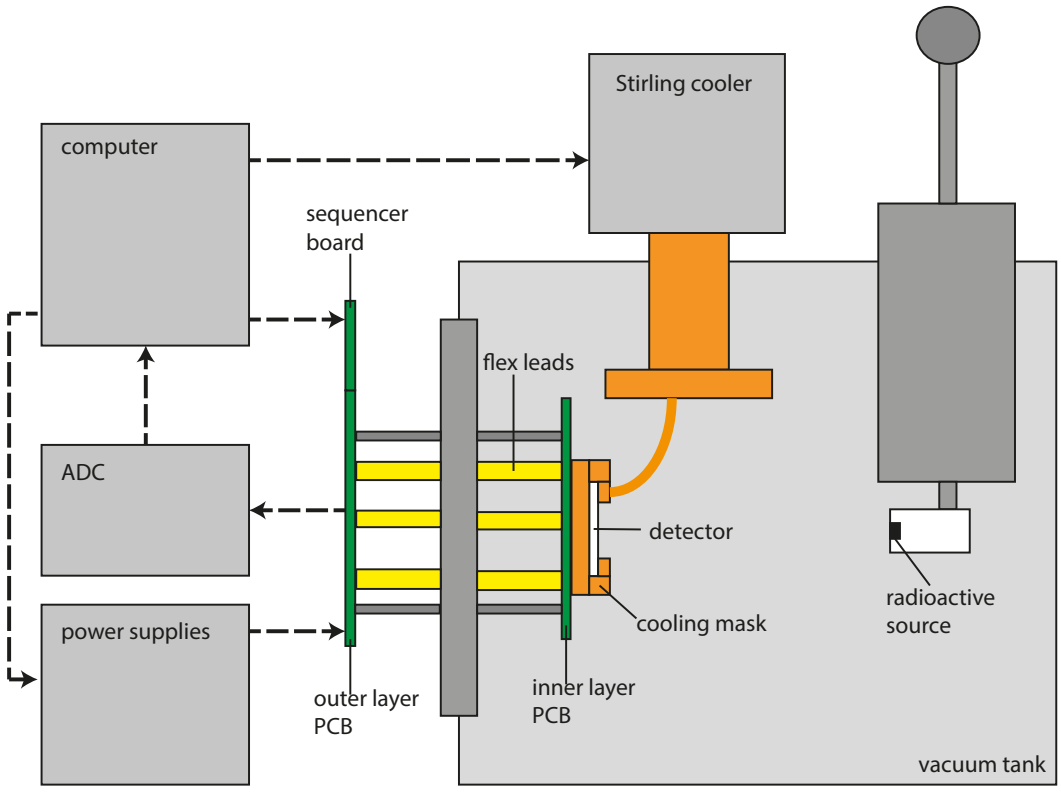


Figure 4.2.2.: Schematic of the spectroscopic setup including the vacuum system, power and digital signal supplies, radiation source, cooling and data processing system.

In order to perform spectroscopic measurements with the DEPFET APS, a complex, newly built setup is needed, see figure 4.2.2 for a schematic drawing. The detector hybrid including DEPFET matrix, the readout and control ASICs, as shown in figure 4.2.1b, is mounted on a Printed Circuit Board (PCB) using a Zero Insertion Force (ZIF) socket inside a steel vacuum tank. The APS needs to be cooled to decrease the measurement noise due to leakage current in the DEPFET bulk caused by thermal generation. For this purpose, the hybrid is contacted by a cooling mask that is connected to a cold head by copper braids. A remotely controlled RICOR K535 Stirling cooler ensures a stable operation temperature of about -60°C, which is monitored with a temperature diode on the IS chip. The temperature was found to vary less than 1°C within a day and within a measurement series.

Digital sequencing signals for ASTEROID and SWITCHER as well as the power signals for ASICs and DEPFET are fed through flex leads and vacuum tight feedthrough integrated in the vacuum flange. Therefore, the newly designed inner and

outer PCB host safety circuits, filtering stages, pull up resistors for digital signals and buffering capacitors for supply lines. The analog output signal of the ASTEROID is also fed out of the vacuum tank through those flex leads. Output buffers on inner and outer PCB reinforce and amplify the signal. On the outer PCB test in- and outputs are implemented as well as a temperature monitoring board, which is connected to the temperature diodes on the DEPFET matrix.

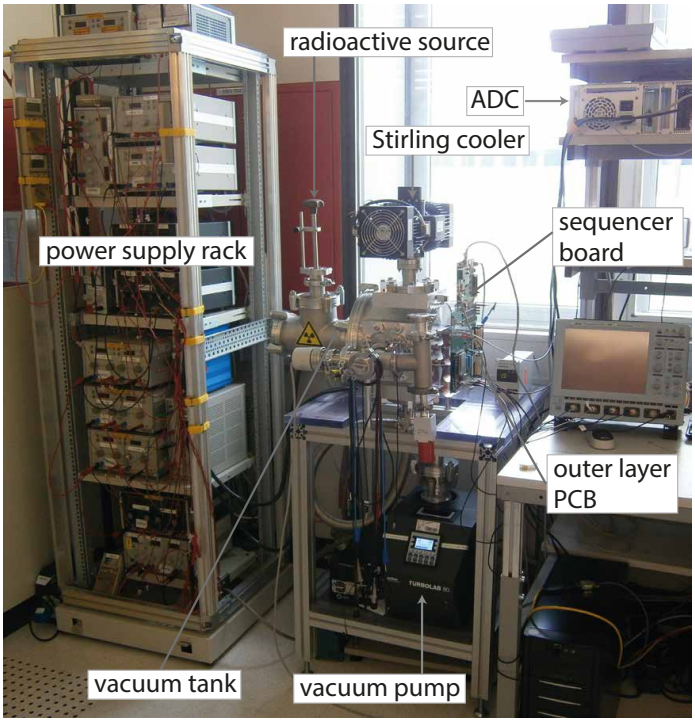


Figure 4.2.3.: Exterior view of the setup for spectroscopic measurements.

The required sequencer signals for the dynamic detector operation are generated by a customized board, the so-called X-Board. This programmable board is connected to the outer PCB via optical couplers for galvanic isolation. The sequencer signals i.a. include a general timing clock, shift register clock for the SWITCHER ASICs and multiplexing clock for the analog output of the ASTEROID readout ASIC. The Analog to Digital Converter (ADC) converts the analog output signal of the ASTEROID into a digital signal, which is then stored on hard disc by a data acquisition computer system. In order to store the information of the pixel position together with the output signal, the whole setup is synchronized by the general timing clock. Therefore, this timing clock from the X-Board is not only connected to the ASICs but also to the ADC and the controlling computer.

An oscilloscope is used to monitor several diagnostic signals of the ASICs and the sequencer signals. Figure 4.2.3 depicts also the power supply rack as well as the vacuum pump. The Oerlikon Turbolab 80 ensures an operating pressure of about $1.4 \cdot 10^{-5}$ mbar in the tank to avoid icing on the cooled detector. With the detector temperature of -60°C and the low pressure in the vacuum tank, operating conditions

sufficiently close to the final operating conditions for the experiment in space are given. In addition, the handling system for the radioactive Mn-Kα_{1+2} source is shown in figure 4.2.3.

4.3. Measurement conditions

In order to start a measurement series, a reference point for the bias voltages must be defined for every design variant. The criteria for the reference bias are:

- the ring V_{R1} and backside potential V_{B} must ensure a fully depleted device for the DEPFET to function properly as discussed in section 2.2.3.
- the drain voltage V_{D} is fixed at -5 V as this value has been chosen for the electrical characterization, see table 3.2.1.
- the current source of the ASTEROID forces $|I_{\mathrm{PMOS}}|$ to 100 µA because this is commonly used for the DEPFET operation as compromise between a high detector gain and sustainable power consumption.
- the gate on potential V_{Gon} is set to a value in the saturation region such that the source potential V_{S} (I_{PMOS},V_{D}) is about -1 V. There are two reasons for the chosen negative V_{S}: The input voltages at ASTEROID have to be between +1.7 V and -1.7 V and the removal of electrons from the internal gate leads to a positive voltage step at the source node. In addition, the voltage shift towards more positive potentials as a result of radiation damage throughout an astronomy mission must be considered during the test period [69].
- the gate off potential V_{Goff} is set to +5 V to inhibit current flow between source and drain completely when rows are in off-state because V_{Th} for all designs is much more negative, see table 3.3.5.
- the clear gate on voltage V_{CGon} is chosen as positive as possible but the difference to V_{Gon} must not be higher than 12 V to keep the risk of an insulator breakdown between overlapping gate and clear gate as low as possible.
- the clear gate off potential V_{CGoff} must be clearly more negative than V_{CGonset} from table 3.3.12.
- the clear on potential V_{Con} is chosen as positive as possible in order to provide a fast clear process. It is limited only by the SWITCHER ASIC [70]. Commonly V_{Con} of about +20 V is used.
- the clear off voltage V_{Coff} needs to be clearly more negative than V_{Conset} from table 3.3.11.
- the inner substrate contact is set to a sufficiently positive voltage V_{InS} in order to drain the surface leakage current of the polysilicon structures.
- the outer substrate contact mentioned in section 2.2.4 is bonded to a ground contact on the detector hybrid.

The chosen reference potentials are listed in table 4.3.1. Note that for gate, clear gate and clear an on as well as an off potential is given because with these contacts the on or off-state of a whole row is controlled and they are connected over the gate and clear SWITCHER ASICs respectively. For the short gate design the source potential V_S is close to 0 V in contrast to -1 V for the other designs. This results from a chosen gate on voltage V_{Gon} that does not push the limits of 12 V difference between gate and clear gate.

	Cut Gate	Quasi Linear	Narrow Gate	Short Gate
V_{R1} [V]	-15	-15	-15	-15
V_{Goff} [V]	5	5	5	5
V_{Gon} [V]	-3.5	-3.5	-2.8	-3.5
V_{CGon} [V]	6	6	6	6
V_{CGoff} [V]	-3.19	-3.19	-3.19	-3.19
V_{Con} [V]	19.6	19.2	19.2	19.2
V_{Coff} [V]	1.6	1.2	1.2	1.2
V_B [V]	-130	-130	-130	-130
V_D [V]	-5	-5	-5	-5
V_{InS} [V]	1	1	1	1
V_S [V]	-0.948	-1.034	-1.198	-0.07

Table 4.3.1.: Reference potentials applied to the DEPFET during spectroscopic measurements.

V_{Goff} and V_{CGon} are fixed during the measurements as no significant influence on the detector performance is expected from their variation. This study concentrates on the variation of the parameter V_{Con}, V_{Coff}, V_{CGoff}, V_{InS}, V_B, V_{R1}, V_{Gon}, V_D and I_{PMOS}. The results of these characterizations are presented in section 4.5.3.

4.3.1. Measurement timing

An other crucial set of measurement parameters beside the biasing conditions is the measurement timing. For Athena increased data throughput is needed and thus, the limits of the measurement speed must be tested. As mentioned in section 4.2.2, all events in the spectroscopic setup are synchronized by the general clock from the X-Board. For all measurements performed in this thesis its frequency is set to 20 MHz. The DEPFET operation time line is shown in figure 4.3.1. The operation starts usually in row one of the detector. The so-called frame trigger (yellow) shows where the data stream of row 64 ends and where row one begins. The readout phases are monitored with the ASTEROID diagnostic pattern (red). This pattern is generated by an exclusive OR combination of the 16 bits of the random access memory words from the ASTEROID. It is programmed to visualize the readout steps.

The gates of all 64 DEPFETs of row one are activated during the first pulse of the ASTEROID diagnostic pattern. The second square pulse marks the first sampling phase t_{Read} with a length of 1 µs described in section 2.2.5. The third pulse illustrates the clear cycle with t_{Clear}. In figure 4.3.1 also the clear and clear gate trigger for the SWITCHER ASICs can be seen. The clear phase is followed by the settling time

t_{Settle} and the second sampling phase t_{Read} of the ASTEROID. The last square pulse marks the sample and hold of the output signal in the readout ASIC. Afterwards, the signal information of row one is multiplexed out to the ADC during t_{Muxout}. The total processing time of the 64 DEPFETs in one row is $t_{\mathrm{Row}} = 13.25$ µs leading to a frame time t_{Frame} of 848 µs for all 64 rows of the IS device.

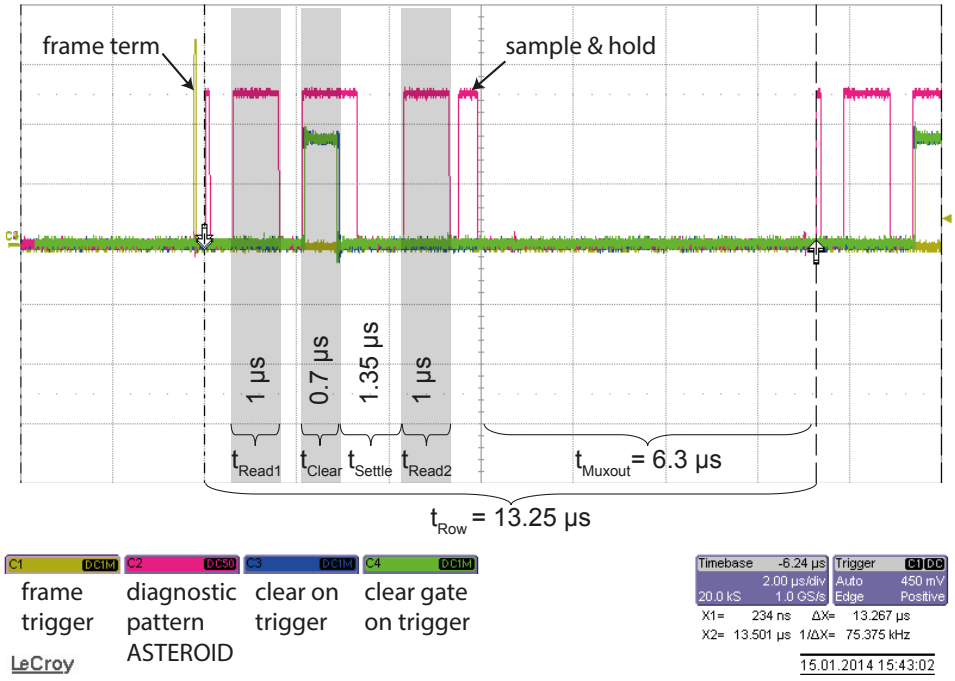


Figure 4.3.1.: Oscilloscope screenshot of the programmed diagnostic pattern from ASTEROID with additional clear, clear gate and frame trigger.

In the frame of this thesis, a variation of t_{Frame}, t_{Clear} and t_{Settle} is investigated. For the variation of t_{Frame} a delay of 100, 300 and 1000 clock cycles of each 50 ns length is inserted at the end of each frame before the frame trigger. Hence, the signal integration time from equation 2.2.40 $t_{\mathrm{Int}} = t_{\mathrm{Frame}}$- t_{Row} is increased for all pixels, as t_{Row} is constant. Due to the extensive accumulation of leakage current in the internal gate, the frame time could not be extended further for this measurements. From these measurements the leakage current of the detector can be determined. The result is presented in section 4.5.1. t_{Clear} and t_{Settle} are also increased by adding clock cycles, which leads to an increase of t_{Frame} as well. If either t_{Clear} of t_{Settle} are shortened, the other time will be extended. Thus, t_{Frame} as well as t_{Row} stay constant. This is done in order to minimize the influence of an increasing leakage current on the detector performance close to the speed limit. On the other hand, extending t_{Clear} and t_{Settle} is not expected to have an impact on the detector performance. Hence, an increase of leakage current is tolerated. The results of the timing variations are discussed in section 4.5.3.

4.3.2. Source potential shift

For the spectroscopic characterization only source follower devices are used with the ASTEROID as readout ASIC. Through the current source of the ASTEROID the current I_{PMOS} is fixed during detector operation. Drain potential V_{D} as well as gate voltage V_{Gon} are set by the SWITCHER and power supplies. Thus, the source potential V_{S} is the only self-adjusting voltage. As the source is the reference point within a transistor, also the varied bias voltages for the spectroscopic characterization are referred to V_{S} potential. Hence, the source potential as well as its shift dependent on parameter variations needs to be determined.

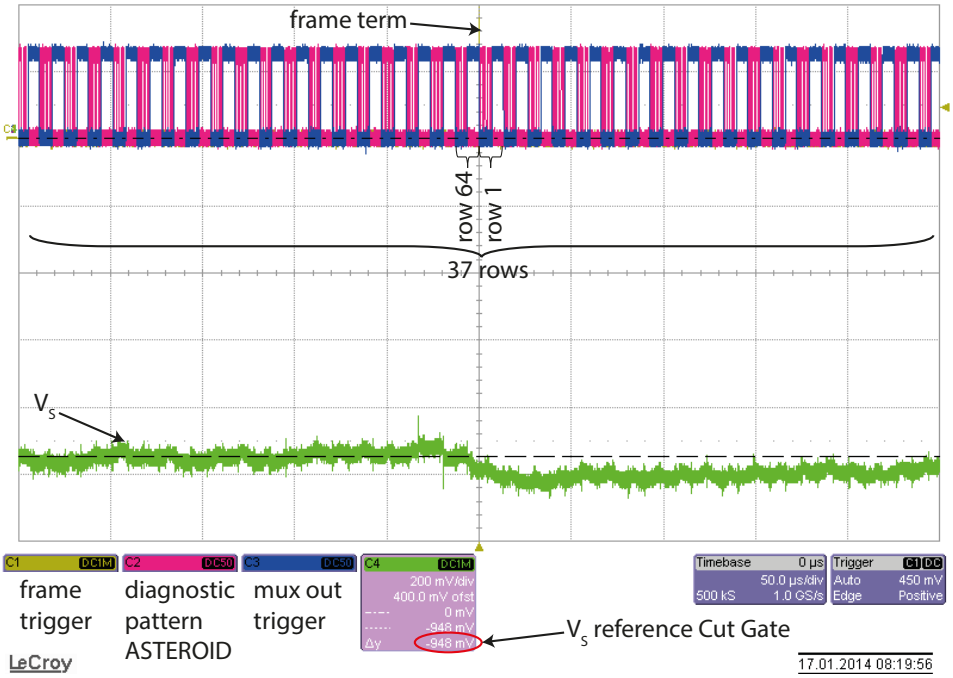
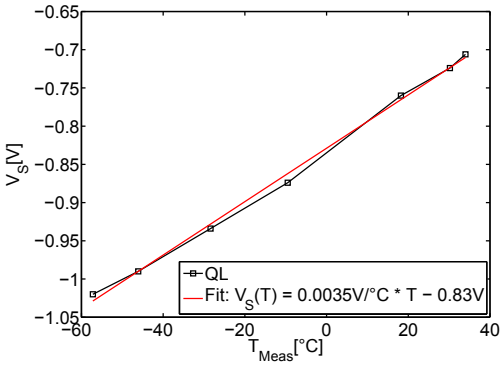


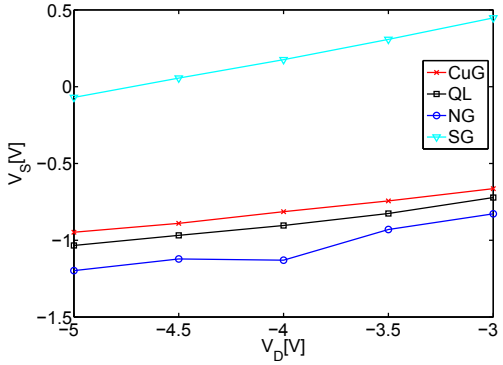
Figure 4.3.2.: Determination of the average source potential V_{S} using an oscilloscope.

It is possible to monitor the source potential V_{S} through a test switch of the ASTEROID using an oscilloscope. The approach is illustrated in figure 4.3.2 for the source potential of column one. It can be seen that the green V_{S} curve fluctuates from row to row within one device. This was expected from the PMOS characteristics deviation due to the production technology presented in section 3.3. The average source potential V_{S} for every device is determined manually using the oscilloscope cursors because during the dynamic operation the access to V_{S} of single pixels is not possible.

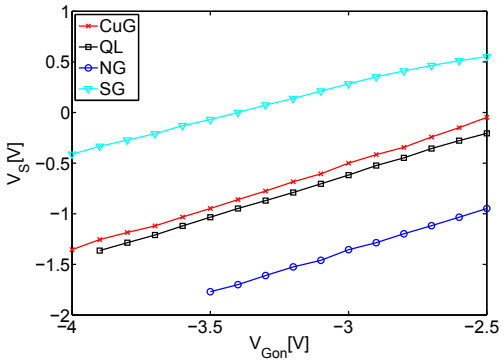
The correlation of the source potential to the other potentials are shown in figure 4.3.3 and parametrized in table 4.3.2. Parameters like the clear potential V_{Con} or V_{Coff} are not mentioned because they have no influence on the source level. It can be seen, that the DEPFET PMOS bias voltages have a stronger influence on the source potential than clear gate, ring or backside bias.



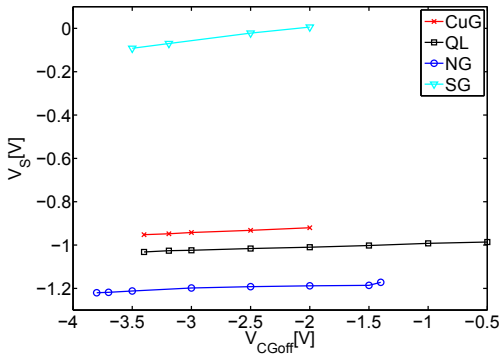
(a) Source potential V_S vs. operation temperature T_{Meas}.



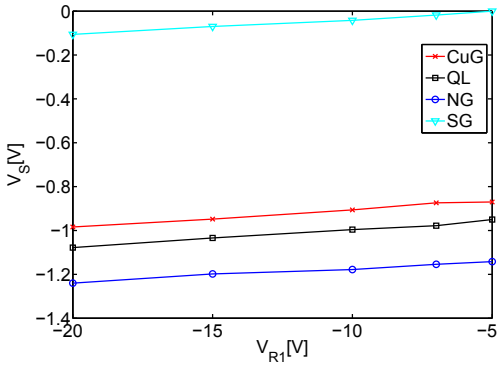
(b) Source potential V_S vs. drain potential V_D.



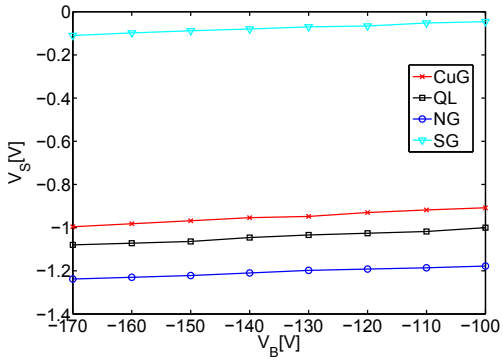
(c) Source potential V_S vs. gate on voltage V_{Gon}.



(d) Source potential V_S vs. clear gate off potential V_{CGoff}.



(e) Source potential V_S vs. ring potential V_{R1}.



(f) Source potential V_S vs. backside voltage V_B.

Figure 4.3.3.: Correlation of the DEPFET PMOS source potential V_S on the operation temperature for the quasi linear design as well as on other bias voltages for all four design variants: QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate, SG = Short Gate.

Due to the capacitive coupling, the slope of V_S (V_D) and V_S (V_{Gon}) vary among the different DEPFET designs. According to the relation of the contact areas A_{CuG} $>A_{QL}$ $>A_{NG}$ $>A_{SG}$, the source potentials V_S (V_{Gon}) vary respectively.

	Cut Gate	Quasi Linear	Narrow Gate	Short Gate
V_S (V_D)	$0.143 \cdot V_D$-0.24	$0.153 \cdot V_D$-0.28	$0.187 \cdot V_D$-0.30	$0.258 \cdot V_D$ +1.21
V_S (V_{Gon})	$0.864 \cdot V_{Gon}$ +2.09	$0.838 \cdot V_{Gon}$ +1.90	$0.825 \cdot V_{Gon}$ +1.11	$0.661 \cdot V_{Gon}$ +2.25
V_S (V_{CGoff})	$0.023 \cdot V_{CGoff}$-0.87	$0.016 \cdot V_{CGoff}$-0.98	$0.017 \cdot V_{CGoff}$-1.15	$0.066 \cdot V_{CGoff}$ +0.14
V_S (V_{R1})	$0.008 \cdot V_{R1}$-0.83	$0.008 \cdot V_{R1}$-0.91	$0.006 \cdot V_{R1}$-1.11	$0.007 \cdot V_{R1}$ +0.03
V_S (V_B)	$0.001 \cdot V_B$-0.78	$0.001 \cdot V_B$-0.89	$0.001 \cdot V_B$-1.09	$0.001 \cdot V_B$ +0.04

Table 4.3.2.: Parametrized source potential correlation of the DEPFET.

During the cooling process of the detectors, the source shifts also with temperature, which is shown exemplarily for the quasi linear design in figure 4.3.3a. Owing to the control loop of the cooling system, the temperature change during a measurement series is less than 1°C leading to a source potential V_S shift of less than 3.5mV. Therefore, V_S is considered as not influenced by temperature during the measurements.

For the comparison of the operation windows for the different DEPFET variants in the results section 4.5.3, the potentials are referred to the source potential and are indicated exemplary as V_{CGoffS} instead of V_{CGoff}. In addition to the measurement series for bias voltages and timing, a variation of I_{PMOS} (V_S =const.) has been done. The source potential is readjusted through a shift of V_{Gon}. The results of these parameter variations and their difference to measurements without V_S readjustment are discussed in section 4.5.3.

4.4. Measurement routine and data analysis

In the last sections the varied voltages and timings as well as the measurement conditions for the spectroscopic characterization have been presented. The measurement procedure used to determine operation windows with stable detector performance for every varied parameter is presented in the following.

4.4.1. Acquisition of a measurement series

First of all, the detector biasing is set to the reference potentials presented in table 4.3.1 as well as the common timing listed in figure 4.3.1 is set. Using the oscilloscope, a rough estimation of the measurement range for the chosen bias voltage is done by monitoring the ASTEROID output and diagnostic signal while varying the potential under test. The first measurement recorded during a series is a Mn-Kα_{1+2} spectrum with applied reference potentials and common timing. The measurement data is analyzed as described later in section 4.4.2. The reference data for all measurement series of a detector are compared among each other in order to ensure detector performance stability over a month of extensive testing. Then the parameter of choice is varied step by step based on the reference value. For every step a spectrum is recorded and analyzed. The measurement series is terminated when one of the following criteria is fulfilled:

- the proper functionality of the readout or control ASIC is compromised, e.g. by input signal levels outside the allowed range.

- the output signal of the ASTEROID leaves the input range of the ADC and could not be readjusted, e.g. by increasing detector gain or offset.
- the functionality of the detector is not given anymore, e.g. when detector volume is not depleted completely or the clear does not empty the internal gate or even injects charge into it.

In all of these cases no Mn-Kα_{1+2} spectrum can be recorded at all and the measurement series is terminated at the actual measurement point.

For the definition of an operation window with stable detector performance two criteria must be met: The functionality neither of the detector nor of the detector periphery may be restricted. In addition, the spectral resolution $FWHM_{\mathrm{Meas}}$ (Mn-Kα_{1+2}) must be less than 150 eV as required for Athena (see table 1.0.1). The figures of merit for all measurement series are ENC_{Meas}, $FWHM_{\mathrm{Meas}}$ (Mn-Kα_{1+2}), $Gain_{\mathrm{Meas}}$ and offset, as they provide extensive information about the quality of a radiation measurement.

4.4.2. Offline data analysis

For the analysis of the spectroscopic measurement data and the determination of the figures of merit, the in-house analysis tool ROOT based Offline Analysis (ROAn) described in [71] is used. In this section a brief overview of the data analysis is given. For a detailed discussion of the applied algorithms, the reader is referred to [72] and for a description of the step implementation and dependencies see [73].

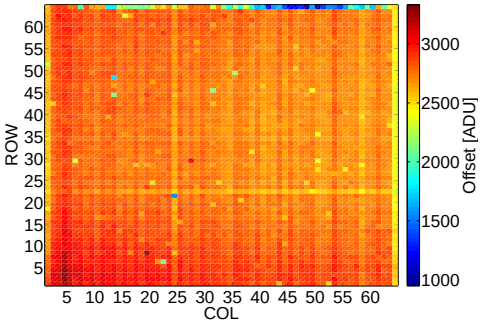
Every measurement data set comprises frames, which are recorded in absence of any radiation. From these so-called dark frames the offset as figure of merit is calculated as mean value over 200 dark frames for each pixel individually.

$$Offset\ [\mathrm{ADU}] = mean(\text{digital output signal [ADU]}) \tag{4.4.1}$$

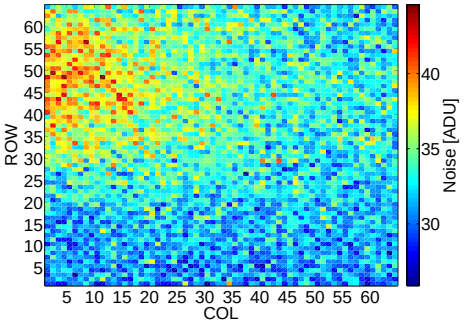
The offset arises from the sum of the DEPFET output signal variation owing to leakage current accumulation and the channel pedestal of the ASTEROID. A typical offset map is depicted in figure 4.4.1a. Then the offset is subtracted from the dark frames. The remaining signal information is corrected for row-effects also referred to as common mode noise. Such noise can e.g. be generated due to pickup from power supplies, computers and other devices in the measurement setup periphery. These effects build row-wise patterns because all pixels within a DEPFET row are read simultaneously by the ASTEROID. After subtracting the offset and the row median from the dark frames any seen variation from zero is due to the pixels noise. A noise value is calculated as standard deviation of the pixel value from the offset for all the dark frames.

$$\begin{aligned} Noise\ [\mathrm{ADU}] = std((&\text{digital output signal [ADU]} - Offset\ [\mathrm{ADU}]) \\ &-\text{common mode [ADU]}) \end{aligned} \tag{4.4.2}$$

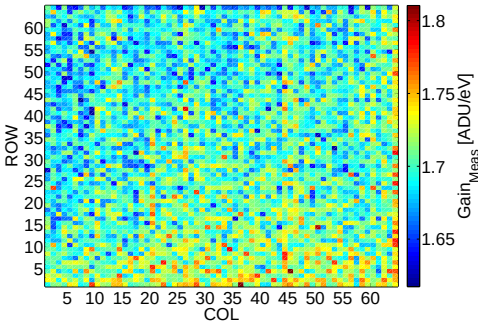
This noise is not yet calibrated, a typical map is shown in figure 4.4.1b.



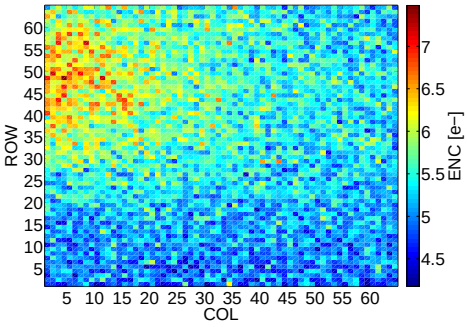
(a) Offset map.



(b) Non-calibrated noise map.



(c) Gain map.



(d) Calibrated noise map.

Figure 4.4.1.: Data analysis result maps for the cut gate (CuG) device F20 of wafer 35 with reference bias conditions.

The offset is subtracted also from the measurement data taken with X-ray radiation, also referred to as illumination frames. Then the common mode correction is performed for these frames as well. Five times the calculated pixel noise is used as threshold for the hit filtering and clustering of events that share common pixel borders. The illumination data set needs to contain between 100 and 150 single events for every pixel, which means hits of Mn-Kα_{1+2} photons with the deposition of the total photon energy in one pixel. Only the single events are used for the pixel-wise gain calculation. For the measurements a radioactive ^{55}Fe source with defined decay is used. The Mn-Kα_{1+2} photons emitted by this source have a defined energy of $E_{\text{Photon}} = 5895$ eV. Thus, the gain is the translation from photon energy in eV to the digital detector output signal in ADU.

$$Gain_{\text{Meas}}\ [\text{ADU/eV}] = \frac{\text{corrected digital output signal photon [ADU]}}{E_{\text{Photon}}\ [\text{eV}]} \tag{4.4.3}$$

The mean gain over all single events per pixel is used for the further data analysis and as figure of merit for the measurement series. Figure 4.4.1c shows the resulting $Gain_{\text{Meas}}$ map of one detector. The gain is used to calculate the calibrated noise. This noise is additionally divided by the electron hole pair generation energy of silicon

$E_{\mathrm{e^-h^+}}$ giving the equivalent noise charge ENC_{Meas},

$$ENC_{\mathrm{Meas}}\ [\mathrm{e^-}] = \frac{\frac{1}{frames}\sum_1^{frames} Noise\ [\mathrm{ADU}]}{E_{\mathrm{e^-h^+}}\ [\mathrm{eV/e^-}] \cdot Gain_{\mathrm{Meas}}\ [\mathrm{ADU/eV}]} \tag{4.4.4}$$

which is displayed in figure 4.4.1d. ENC_{Meas} is taken also as figure of merit.

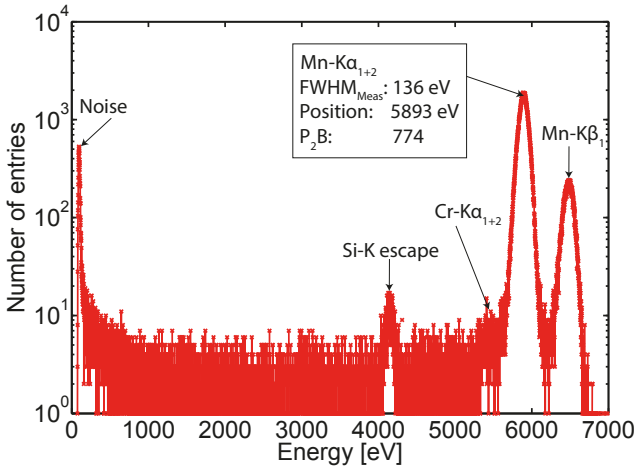


Figure 4.4.2.: Single event spectrum for the cut gate (CuG) device F20 of wafer 35 including calculated peak position, energy resolution $FWHM_{\mathrm{Meas}}$ and P_2B for the Mn-Kα_{1+2} peak.

Using $Gain_{\mathrm{Meas}}$ the digital signal for every pixel and frame is calibrated. The frequency distribution or histogram of the calibrated pixel signals, also called spectrum, is depicted in figure 4.4.2. For this spectrum only the information of single events, meaning hits that do not share charge with surrounding pixels, are used. Spectra can also be created for all valid events including singles with no charge sharing, doubles with charge sharing between two neighboring pixels, triples and quadruples respectively.

In figure 4.4.2 besides the Mn-Kα_{1+2} line, the Mn-Kβ_1 line of the radiation source, the Si-escape peak as well as a faint fluorescence peak Cr-Kα_{1+2} of the chromium-nickel steel vacuum chamber can be seen. Owing to the detectors energy resolution Mn-Kα_1 with E_{Photon} =5898.75 eV and Mn-Kα_2 with E_{Photon} =5887.65 eV fuse into one peak at a position of 5895 eV. This peak is approximated by a Gaussian fit. The full width at half maximum of this fit equals the energy resolution $FWHM_{\mathrm{Meas}}$, which is also used as figure of merit for the measurement series. Additionally, the peak-to-background ratio P_2B, which is the ratio from peak height of Mn-Kα_{1+2} to the mean background height between 800 and 1200 eV, and the calibration accuracy are provided in the fitting model. The peak position of Mn-Kα_{1+2} should be at 5895 eV and it is fitted as 5893 eV for the measurements, which stands for a calibration tolerance of 0.03% at this photon energy.

4.4.3. Accuracy of the offline analysis

The literature for ROAn [71, 72, 73] does not provide an estimation of the analysis error. The standard deviation of the input signal for ROAn, which is equal to the digital output signal of the measurement setup, is given by the measurement noise from equation 4.4.2. The figures of merit $Offset$, ENC_{Meas}, $Gain_{\mathrm{Meas}}$ and $FWHM_{\mathrm{Meas}}$ are calculated out of this signal as average values over 200 dark frames or 150 single events per pixel, respectively. As calculating the error of these mean values using

$$\text{Error of mean} = \frac{\text{Error per measurement point}}{\sqrt{\text{Number of measurement points}}}$$

leads to negligible errors, the stability over time and the repeatability of the reference measurements is used as measure for the accuracy of the spectroscopic characterization.

Device	Cut Gate PXD7 W35 F20	Quasi Linear PXD7 W35 E01	Narrow Gate PXD7 W35 F01
period of testing [month]	3	2	2
number of reference measurements	13	12	13
σ ENC_{Meas} [e^-]	0.03	0.02	0.02
σ $Gain_{\mathrm{Meas}}$ [ADU/ eV]	0.0007	0.0006	0.0004
σ $FWHM_{\mathrm{Meas}}$ [eV]	0.33	0.26	0.30
σ Offset [norm. Ref]	0.0030	0.0041	0.0019

Table 4.4.1.: Deviation of the figures of merit for the reference biasing condition over the period of testing.

A spectroscopic measurement with reference biasing conditions was made several times during the period of testing for every detector. The deviation of the figures of merit for the reference measurements is listed in table 4.4.1. In the following sections as well as in the corresponding appendix A.2, no error bars will be shown but only parameter changes, which are larger than the deviation, are discussed as significant.

4.5. Results of spectroscopic measurements

First the new measurement setup is qualified in sections 4.5.1 and 4.5.2. Afterwards the spectroscopic performance of the four DEPFET designs is characterized in section 4.5.3 for bias voltage and timing variations. There, also the operation window size for stable detector operation is defined for each parameter as well as the comparison with the predictions from the electrical measurements is done. Finally, the electrical qualification and the spectroscopic data are combined to reveal the charge transconductance g_{q} of the DEPFET variants in section 4.5.4. The assessment of the operation window for the different DEPFET designs is given in section 4.6.

4.5.1. Leakage current

As shown in the figure 4.4.2 for the cut gate device F20 from wafer 35, the measured energy resolution $FWHM_{\text{Meas}}$ is 136 eV. This is not as good as expected. For similar DEPFET designs with a pixel size of 75 × 75 µm^2 a $FWHM_{\text{Meas}}$ of 127 eV has been demonstrated using the same ADC and ASTEROID as readout ASIC [13]. According to equation 2.2.41, the energy resolution of the detector is given by

$$FWHM = 2.355 \cdot E_{\text{e-h+}} \cdot \sqrt{ENC^2_{\text{Filter}} + N^2_{\text{Leak}} + Fano^2}$$

The calibrated noise of a measurement ENC_{Meas} comprises of

$$ENC^2_{\text{Meas}} = ENC^2_{\text{Filter}} + N^2_{\text{Leak}}$$

Following equation 2.2.35, the equivalent noise charge of the DEPFET and filter combination ENC_{Filter} is similar for the measurement discussed in [13] with the old setup and the current measurements. The Fano noise is also assumed as fixed because the wafer material and photon energy are similar, too. Hence, according to equation 2.2.40, the remaining noise contribution comes from the leakage current. This noise equals the dispersion of the Poisson distribution for I_{Leak} and can be written as

$$N_{\text{Leak}} = \sqrt{I_{\text{Leak}} \cdot t_{\text{int}}}\ [e^- \text{rms}]$$

Thus, the first measurement series concentrates on a variation of the frame time t_{Frame} and the integration time t_{Int}. Plotting the squared ENC_{Meas} versus t_{Int} as shown in figure 4.5.1, gives the leakage current I_{Leak} in $[\frac{e^-}{\mu s \cdot \text{pixel}}]$ as slope of the resulting curve because of

$$ENC^2_{\text{Meas}} = ENC^2_{\text{Filter}} + I_{\text{Leak}} \cdot t_{\text{int}}$$

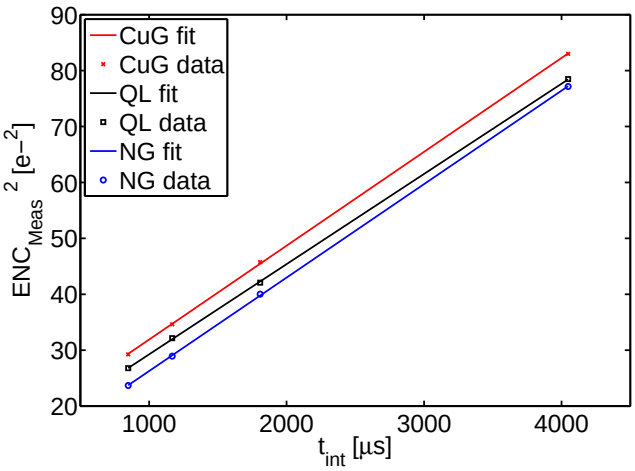


Figure 4.5.1.: Squared equivalent noise charge for varied integration times t_{Int} measured for three designs. The slope of the curve equals the leakage current I_{Leak} and is given in table 4.5.1. QL = Quasi Linear, CuG = Cut Gate, NG = Narrow Gate.

The measurement series could not be performed for the short gate device, as will be explained in section 4.5.3. The remaining three designs show a similar slope and I_{Leak} respectively. The results are summarized in table 4.5.1.

	Cut Gate	Quasi Linear	Narrow Gate
T_{Meas} [°C]	-59.6	-57.5	-57.0
I_{Leak} $[\frac{e^-}{\mu s \cdot \text{pixel}}]$	0.0168	0.0161	0.0167

Table 4.5.1.: Leakage current for three different DEPFET designs.

The leakage current I_{Leak} of the cut gate device is with 0.0168 $\frac{e^-}{\mu s \cdot \text{pixel}}$ slightly larger than 0.0161 $\frac{e^-}{\mu s \cdot \text{pixel}}$ of the quasi linear and 0.0167 $\frac{e^-}{\mu s \cdot \text{pixel}}$ of the narrow gate designs. Nevertheless, inserting I_{Leak} from table 4.5.1 in equation 2.2.40 gives for all three designs $N_{\text{Leak}} = 3.8$ e-. Adding $ENC_{\text{Filter}} = 4.7$ e- for the ASTEROID according to equation 2.2.35 calculated with the parameters provided in section 2.2.5 and the Fano noise of 13.7 e- from section 2.1, gives an expected $FWHM_{\text{Meas}}$ of about 130 eV for the current detector and setup combination. The reason for the increased $FWHM_{\text{Meas}}$ of 136 eV in comparison to the expected 130 eV will be revealed in the following section.

4.5.2. Influence of a variation of deep n implantation on the performance

Device	P05 W80 H01	P05 S80 A07	P07 W35 I02	P07 W35 F20
Production run	5	5	7	7
Pixel size	75×75µm^2	75×75µm^2	75×75µm^2	100×100µm^2
Design type	CuG	CuG	CuG	CuG
Deep n-doping	DN1	DN0/2	DN0/2	DN0/2

Table 4.5.2.: Characteristics of the DEPFET detectors used for the setup qualification.

The simplest way to test whether the DEPFET design, the production technology or the measurement setup impair the energy resolution, is to operate detectors produced with different production technologies and detector sizes with the new setup. Four different DEPFET modules are chosen and their production parameters are listed in table 4.5.2. The first detector is the well known 64 × 64 DEPFET matrix from a former production with 75 × 75 µm^2 pixel size referenced with P05 W80 H01. The second device is taken also from the former production and has the same pixel size but a difference in production technology and it is called P05 S80 A07. The technology difference lies in the deep n-doping that is essential for the formation of the internal gate. From the DEPFET production of the IS devices also a matrix with 75 × 75 µm^2 pixel is available (chip P07 W35 I02). Lastly, the cut gate IS device with 100 × 100 µm^2 pixel size (chip P07 W35 F20) is taken.

The deep n-doping variants are illustrated in figure 4.5.2. The total dose of the deep n-doping can be reached in two ways. Either it is implanted in one step within the polysilicon ring (DN1) or as a two step process with a light dose implanted over

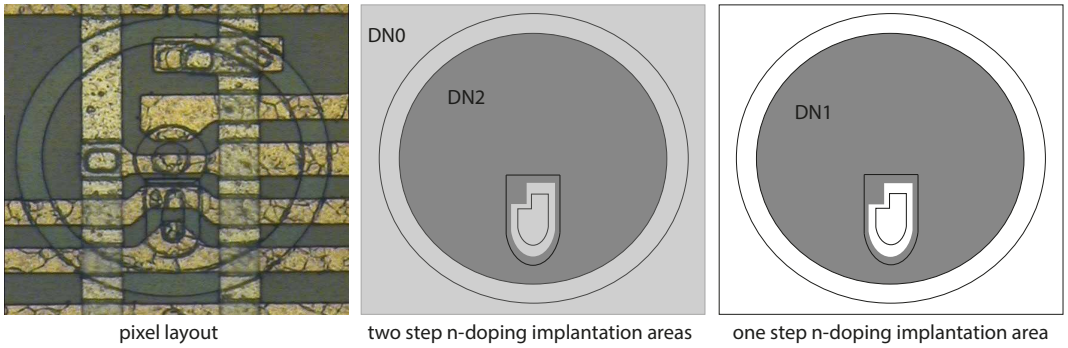


Figure 4.5.2.: Deep n-doping variants. The gray color marks the implantation areas. For DN0 the implantation covers the whole pixel area. DN1 or DN2 are implanted within the polysilicon ring and without the clear contact area.

the whole pixel area (DN0) and the major dose implanted within the polysilicon ring (DN2). Note that all IS devices are produced with the two step implantation process.

The measurement conditions of the four detectors with distinct properties and the measurement results for I_{Leak} and $FWHM_{\mathrm{Meas}}$ are listed in table 4.5.3. The biasing was chosen such that the source potential V_{S} of all devices is about -1 V. For all chips the leakage current I_{Leak} has been determined with the test procedure discussed in section 4.5.1. In table 4.5.3 can be seen that for the smaller pixel size, independently of production technology or batch, I_{Leak} was found to be lower than for the IS device. There is no reason known for that. Additionally, for all detectors an energy resolution $FWHM_{\mathrm{Meas}}$ below 130 eV would be expected according to equation 2.2.41

$$FWHM = 2.355 \cdot E_{\text{e-h+}} \cdot \sqrt{ENC^2_{\mathrm{Filter}} + N^2_{\mathrm{Leak}} + Fano^2}$$

but this could only be reached for the device with DN1. The theoretical value $FWHM_{\mathrm{Theo}}$ calculated with the ENC_{Meas} taken from the spectroscopic measurements differs for all chips from $FWHM_{\mathrm{Meas}}$. This indicates the presence of an additional deviation factor. Thus, equation 2.2.41 has to be enhanced to

$$FWHM = 2.355 \cdot E_{\text{e-h+}} \sqrt{ENC^2_{\mathrm{Filter}} + N^2_{\mathrm{Leak}} + Fano^2 + Loss^2} \qquad (4.5.1)$$

The additional noise contributor must be signal charge loss before the electron collection in the internal gate because the hybrid and setup periphery is the same for all tested devices.

The statistical charge loss from the charge cloud with N = 1602 e^- calculated using equation 2.1.2 for one Mn-Kα_{1+2} photon lies between 1.9^2 e^- for the device with DN1 and 5.9^2 e^- for those with DN0/2. This is a charge loss of less than 2.3% for all DN0/2 chips, which is attributed to the DEPFET. Nevertheless, the small deviation has a huge impact on the energy resolution because the detector system has a near Fano-limit resolution.

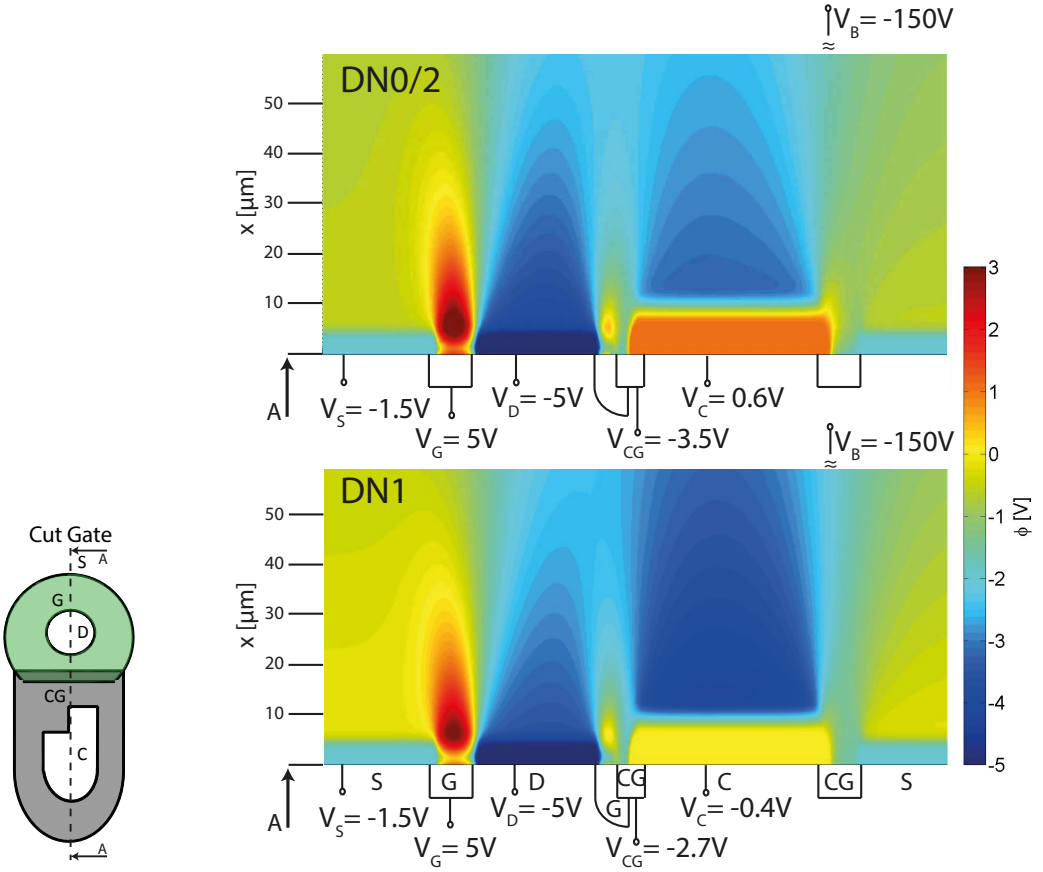
Device	P05 W80 H01	P05 S80 A07	P07 W35 I02	P07 W35 F20
Pixel size	75×75µm^2	75×75µm^2	75×75µm^2	100×100µm^2
Deep n-doping	DN1	DN0/2	DN0/2	DN0/2
V_{R1} [V]	-15	-15	-15	-15
V_{Goff} [V]	+5	+5	+5	+5
V_{Gon} [V]	-4	-3.5	-3.8	-3.5
V_{CGon} [V]	+5	+6	+5	+6
V_{CGoff} [V]	-2.71	-3.5	-3.5	-3.19
V_{Con} [V]	+19	+20.6	+21.2	+19.6
V_{Coff} [V]	-0.4	+0.6	+1.2	+1.6
V_{B} [V]	-140	-130	-130	-130
V_{D} [V]	-5	-5	-5	-5
T_{Meas} [°C]	-40.0	-41.0	-42.0	-59.6
I_{Leak} [$\frac{e^-}{\mu s \cdot \mathrm{pixel}}$]	0.0052	0.0049	0.0049	0.0167
I_{Leak} [$\frac{\mathrm{nA}}{\mathrm{cm}^2}$] @ 20°C	6	6	7	71
ENC_{Meas} [e-]	4.50±0.29	4.66±0.31	5.39±0.42	5.41±0.45
$FWHM_{\mathrm{Meas}}$ [eV]	128	135.2	136.7	135.4
$FWHM_{\mathrm{Theo}}$ [eV]	126.9	126.8	126.8	129.8
Loss [e-]	1.9	5.4	5.9	4.4

Table 4.5.3.: Parameters of the different cut gate DEPFET detectors.

In order to identify the root cause of the charge loss, simulations have been done for the cut gate DEPFET design. In contrast to the simulations discussed in section 2.4, a device thickness of 450 µm has been assumed. The linear cut sections of figures 4.5.3 and 4.5.4 are broadened instead of rotated to imitate a three dimensional structure. The simulations are performed for the two step deep n-doping process as well as the one step technology with the same voltages as used during the measurements. The first cut section (A) depicted in figure 4.5.3a includes the PMOS and NMOS transistor of the DEPFET. The resulting potential distribution along A is shown in figure 4.5.3.

Due to the different n-doping procedures, the clear and clear gate contacts need different bias respectively in order to function properly. For the DN0/2 doping these contacts are biased more positive. The clear structure as well as the PMOS are in off-state in order to simulate the state of the DEPFET during charge collection. For both n-doping variants no potential drop for electron draining is evidenced by simulation cut A.

The second simulation cut B is shown in figure 4.5.4a and the corresponding potential distribution in 4.5.4b. For the second simulation the same biasing conditions for charge collection are used as for cut section A. For DN1 a good potential shielding of about 1 V for the clear contact towards the bulk exists. This barrier is weakened to 0.2 V for DN0/2 on one side of the clear contact. The single sided effect occurs due to the tilt angle used for the implantation process and the intricate alignment of the clear gate polysilicon with the implantation mask.



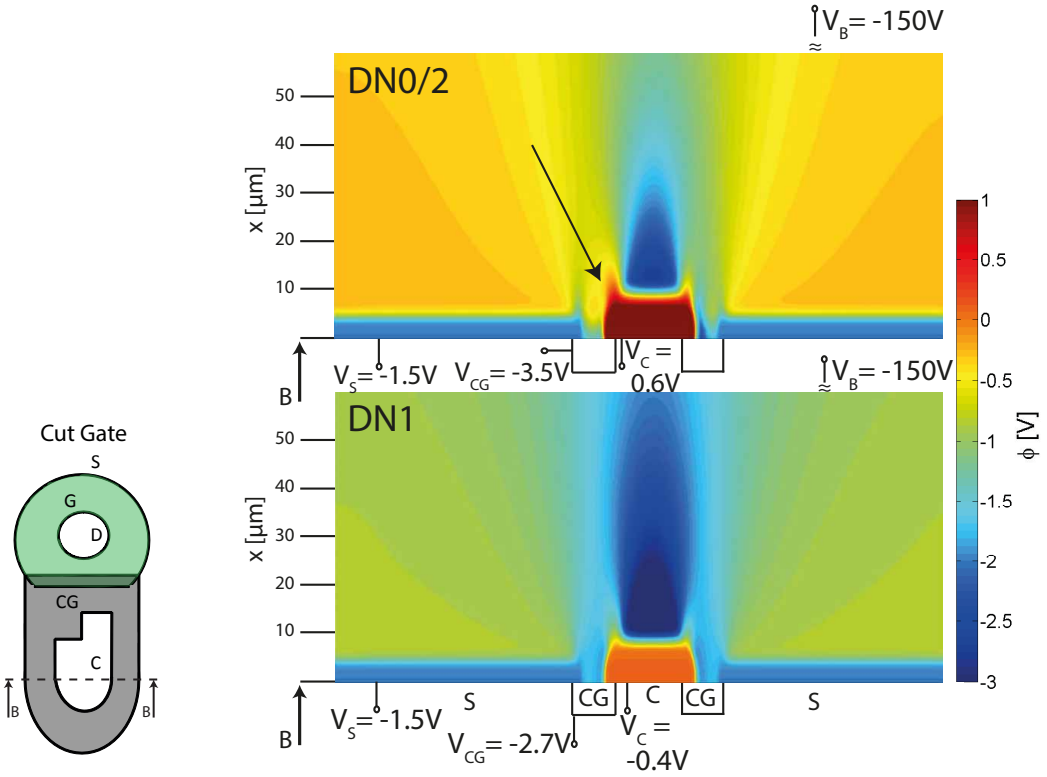
(a) Simulation cut A.

(b) Potential distribution for simulation cut A.

Figure 4.5.3.: The potential distribution in the DEPFET for simulation cut A for the deep n-doping in DN0/DN2 as well as DN1 variant show no electron draining contact.

According to the Boltzmann distribution, 2.3% of electrons can overcome a potential barrier of 0.2 V [74], which is in accordance with the loss during the measurements. If a photon hits the detector in a way that the charge cloud has to drift around the clear contact to reach the internal gate, electrons can be drained into the clear. The difference of 0.5 lost electrons between device P05 S80 A07 and P07 W35 I02 is likely to occur owing to different wafer materials used for the two production runs. A slightly higher bulk doping can cause a further barrier lowering as the implantation procedure uses the same total dose for both production runs.

The newly build measurement setup including periphery, hybrid and ASICs has been validated by achieving the expected energy resolution $FWHM_{\mathrm{Meas}}$ of 127 eV for the well known cut gate device P05 W80 H01 from the former production. In addition, a production technology weakness has been revealed. For further DEPFET productions the single step deep n-doping (DN1) is recommended to keep the energy resolution close to the physically given Fano-limit. Another possibility is to increase



(a) Simulation cut B.

(b) Potential distribution for simulation cut B.

Figure 4.5.4.: The potential distribution of the simulation cut B discloses a weak potential barrier between bulk and clear contact for the DN0/2 doping variant.

the dose of the deep p implantation below the clear contact in order to increase the potential barrier when DN0/2 is used. Nevertheless, the comparison of the spectroscopic performance for the four DEPFET designs with respect to large and stable operation windows, is presented in the next sections.

4.5.3. Comparison of DEPFET designs

	Cut Gate	Quasi Linear	Narrow Gate	Short Gate
$FWHM_{\mathrm{Meas}}$ (single events) [eV]	135.6	134.8	134.8	252.1
P_2B (all events)	1646	1551	1520	428
ENC_{Meas} [e-]	5.42	5.18	4.80	4.31
$Gain_{\mathrm{Meas}}$ [ADU/eV]	1.70	1.79	1.74	1.47

Table 4.5.4.: Quality parameters of the best spectra.

All four DEPFET design variants were produced using the DN0/2 technique. Hence, it is obvious that all designs are expected to achieve an energy resolution $FWHM_{\mathrm{Meas}}$ broader than 130 eV. The measurement result with the narrowest $FWHM_{\mathrm{Meas}}$ for single events are listed in table 4.5.4 for the different DEPFET variants. These data sets have been determined after all measurement series for the biasing voltages were

done. The corresponding histograms of all valid events are depicted in figure 4.5.5.

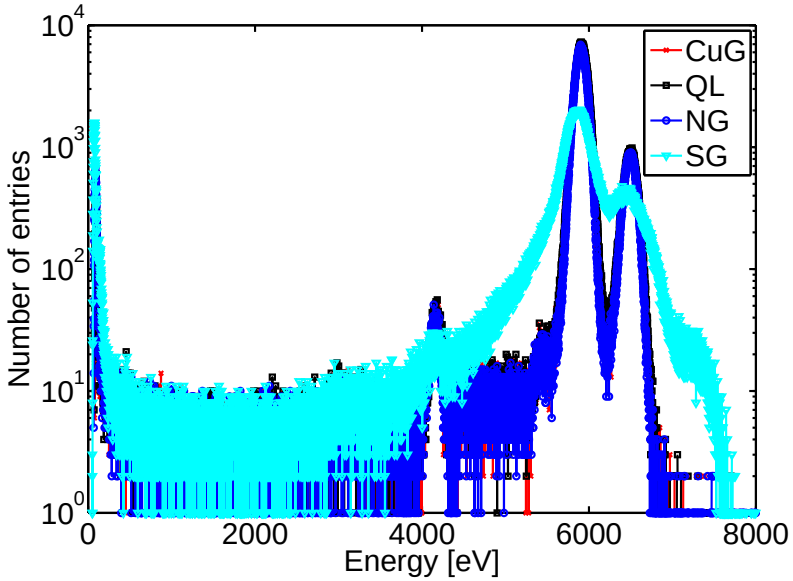
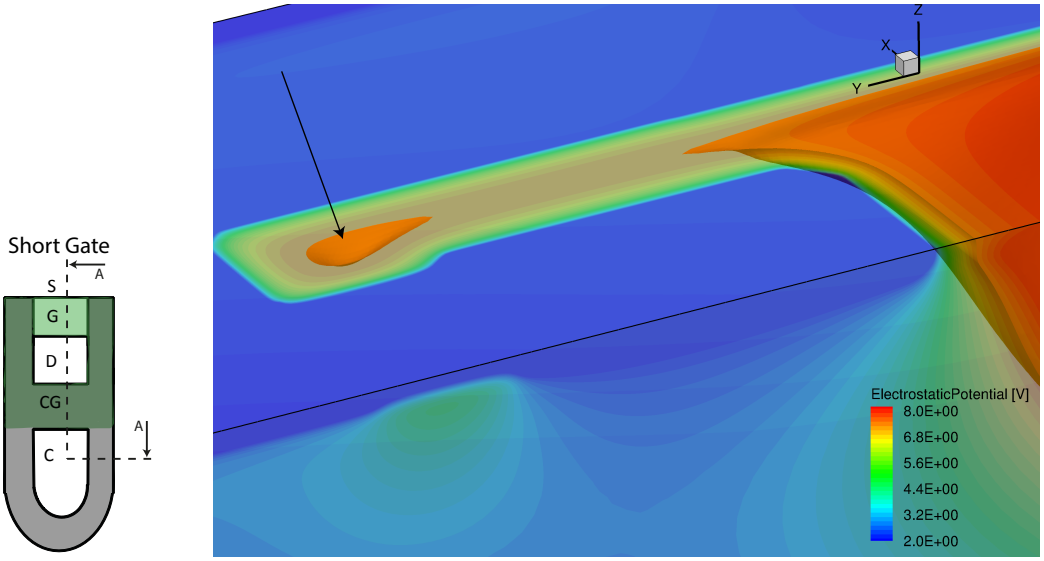


Figure 4.5.5.: Histogram of all valid events for narrowest energy resolution of the Mn-Kα_{1+2} peak for all designs.

It is obvious that the short gate design has the broadest peak and therefore the worst energy resolution $FWHM_{\text{Meas}} = 252.1$ eV of all design variants. The spectra of cut gate, quasi linear and narrow gate design are comparable as they have a similar $FWHM_{\text{Meas}}$ and peak-to-background P_2B.

A peak broadening can occur due to incomplete signal charge collection in the internal gate, as discussed in section 4.5.2 for DN0/2 doping, or an incomplete clear process. The clear is considered as not complete when a part of the collected signal electrons remains in the internal gate. These electrons are added to the signal information during the next readout phase. This leads to a false hit recognition and additional noise contribution owing to a fluctuation of the exact number of remaining electrons.

A three-dimensional simulation of the potential distribution during the clear process has been performed for the short gate design and is shown in figure 4.5.6. It can be seen that the clear potential reaches the internal gate and empties it completely. But some electrons accumulate in a potential pocket below the gate close to the internal gate instead of being drained through the clear contact. After the clear is back in its off-state, the internal gate is the most positive potential and attracts these electrons, that have not reached the clear contact owing to being trapped in the potential pocket. According to the simulations, the potential pocket cannot be minimized by applying other potentials at clear, clear gate or gate. Only the absolute level but not the depth of the pocket varies with different biasing conditions. The amount of



(a) Simulation cut.

(b) Isopotential areas during the clear process.

Figure 4.5.6.: The 3D simulation of the potential distribution during the clear process in the short gate design (picture provided by [75]).

electrons going back and forth between the pocket and the internal gate affects the signal information and adds readout noise.

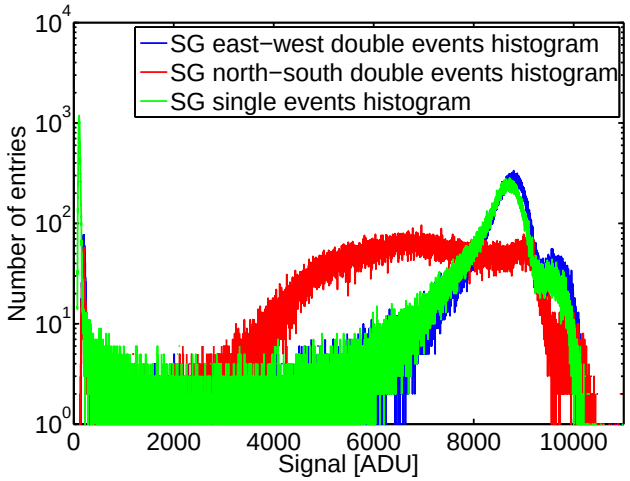


Figure 4.5.7.: Histogram of the non-calibrated measurement data for the short gate (SG) design separated for single events as well as double events.

A closer examination of the measurement data using ROAn revealed that the peak broadening for the short gate design is more distinct for split events than for singles. The non-calibrated histograms for single events and the two types of doubles are

shown in figure 4.5.7. The difference between east-west and north-south splits in the perspective of the detector is illustrated in figure 4.5.8.

When a photon is absorbed in the detector bulk, the charge is forced to the surface of the device by the potential distribution due to the sidewards depletion as explained before in figure 2.2.10. Assuming the charge cloud overlaps the border of two neighboring pixels, it is split because of the potential gradients towards the internal gates as depicted in figure 4.5.8. The internal gate exists only below the PMOS gates and is marked orange in the figure. The electrostatic attraction from the internal gate is weak due to the lateral distance in case of a north-south split. The electrons must diffuse around the clear and during diffusion charge is trapped in the clear contact owing to the production technology discussed in section 4.5.2. On the other hand for the east-west splits a sufficient attraction of the signal electrons towards the internal gate is given. Additionally, their drift path does not pass by the clear contact, which eliminates charge loss. The difference in the mechanisms for charge accumulation is clearly visible in the histograms from figure 4.5.7 for the different types of split events. The peaks for north-south splits are significantly broader compared to singles and east-west splits.

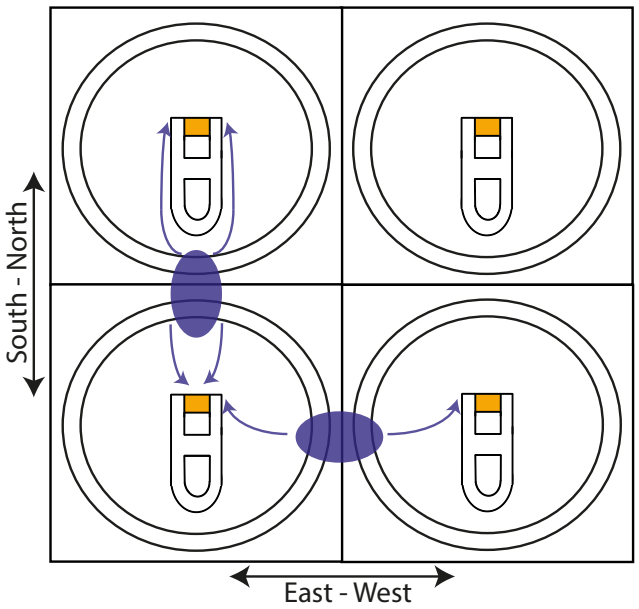


Figure 4.5.8.: Split event clustering for a short gate (SG) matrix with 2 × 2 pixels. The internal gate (iG) is located below the gate, which is marked orange here. The blue area and arrows symbolize the signal charge cloud and the direction of movement near the device surface of the electrons towards the internal gate (iG).

Applying a more positive potential to the backside of the device may improve the energy resolution. In case of split events, the charge cloud is divided in more distance to the surface and the electrons should diffuse into the internal gate without charge loss. The backside potential was found to be not able to compensate the effect as the device is not fully depleted for too positive voltages. The inaccuracy of a

measurement with the short gate design caused by the potential pocket and the charge loss leads to an exclusion of this DEPFET design from all measurement series. The design first must be improved before it makes sense to examine effects of varied bias voltages or timing differences. It is suggested to round off the edges of the gate and clear gate. Hence, the influence of source and drain potential are similar at every point of the overlapping area and the potential pocket is expected to vanish.

Operation window

So far, the new measurement setup has been validated, the influence of the detector leakage current on readout noise and achievable energy resolution has been determined as well as the general functionality of the DEPFET designs has been tested in sections 4.5.1 and 4.5.2. Some of the major findings were a not optimal choice of production parameters and the poor performance of the short gate design.

In the following, the operation window with stable spectroscopic performance for the clear gate off voltage V_{CGoff} is determined exemplarily for all biasing voltages. For the results of all other voltage variations the reader is referred to the appendix A.2.1. Note that the assessment of the operation windows for the different DEPFET designs is given in section 4.6.

As mentioned in section 4.4.1, before recording spectroscopic data, the measurement range for the biasing voltage V_{CGoff} is estimated using the monitoring oscilloscope. The state of the DEPFET cannot be monitored directly but via the output signal of the ASTEROID, which is a mirror of the difference between the DEPFET source potential V_{S} with and without filled internal gate. A typical oscilloscope screen shot for the cut gate device is shown in figure 4.5.9.

The magenta colored digital signal is the programmed diagnostic pattern of the ASTEROID, which was used before in section 4.3.1 to explain the timing of the DEPFET readout. The blue colored digital signal is the multiplexing trigger for the ASTEROID. During its high level (blue phase), the signal read out of the current row is multiplexed out. This output signal of the readout ASIC is shown in green. Each pixel has an individual offset level owing to production, wafer material and temperture distribution conditioned amounts of leakage current for every DEPFET. In section 3.3 with the electrical qualification has been shown, that neither the bulk doping nor the polysilicon structures are constant within a device.

The ASTEROID channel pedestals are added to the resulting pixel offset and form the total offset of a readout node. As explained in section 4.4.2, the offset is corrected for each pixel individually through the analysis software. A change of the source potential V_{S}, e.g. caused by an absorbed photon, influences the output signal directly as depicted in figure 4.5.9 (b). While the ASTEROID processes the signal input from the DEPFET, the output signal (green) shows the ASTEROID last multiplexing potential.

As described in section 4.3.2, a clear gate off potential V_{CGoff} shift does change the

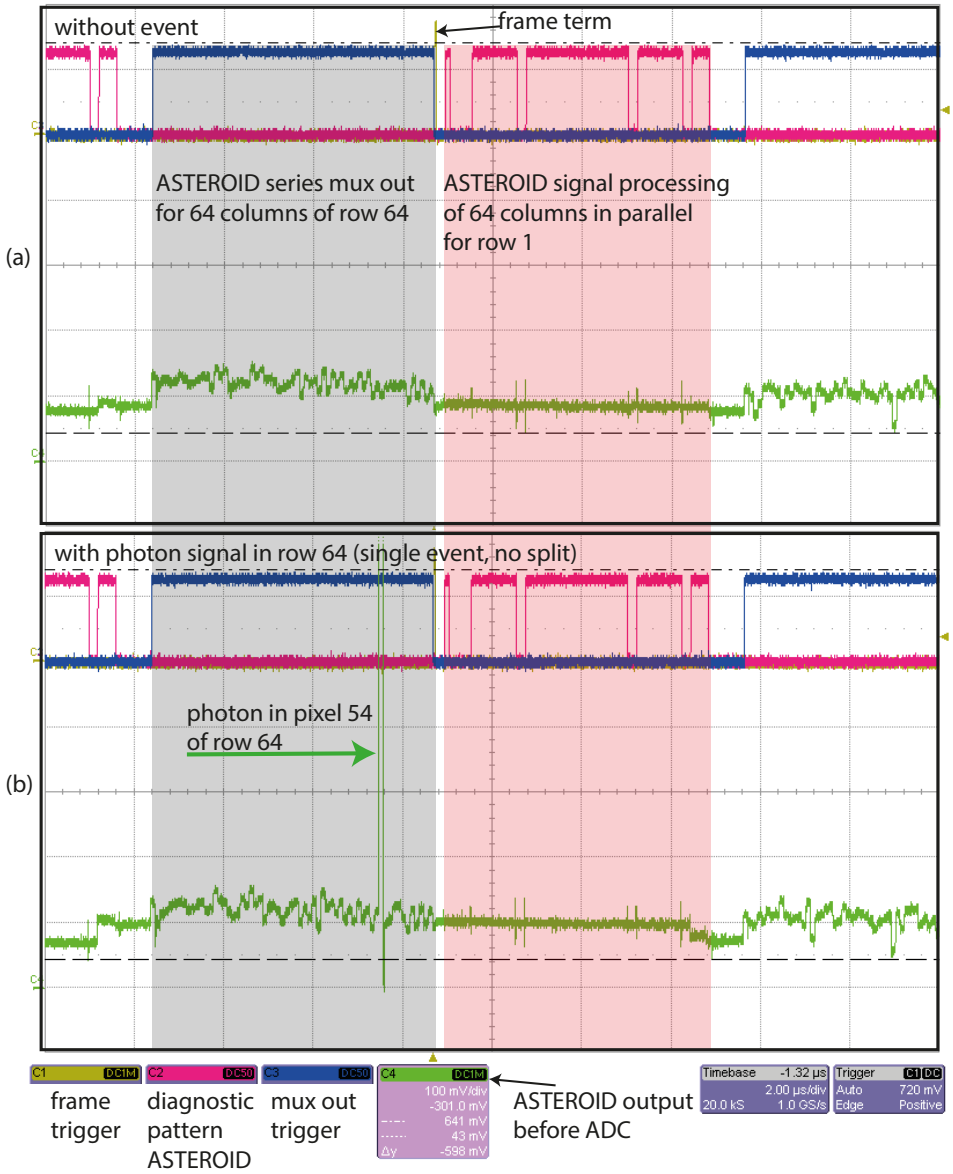
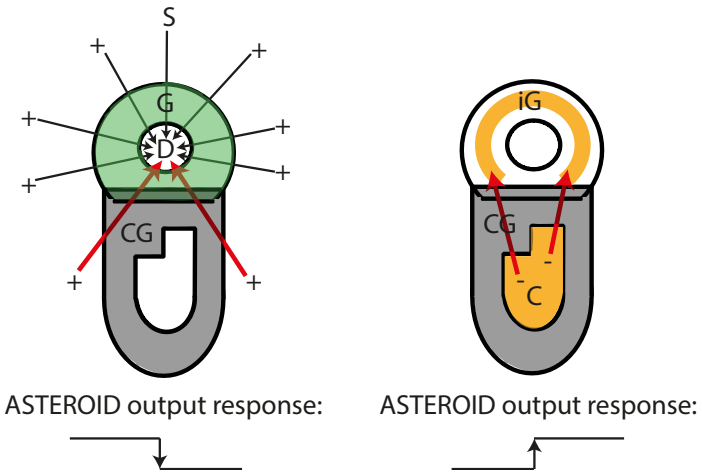


Figure 4.5.9.: Oscilloscope screenshot of the ASTEROID output signal (green) of row 64 (a) without and (b) with photon signal for the cut gate (CuG) detector. During the multiplexing phase (blue) of the ASTEROID, the analog equivalent of the difference between the DEPFETs source potential with and without filled internal gate of all 64 columns of row 64 can be seen. While the ASTEROID processes the DEPFET signal (red phase), the output signal of the ASTEROID stays at its last multiplexing potential.

source potential slightly. However, for the phenomenological estimation of the measurement range, two other effects are used. When V_{CGoff} becomes too negative, holes can flow below the clear gate from drain to source as depicted in figure 4.5.10a. This leads to a drop of the current density in the PMOS because the readout ASIC forces a constant current of 100 µA through the DEPFET. Thus, the source potential V_{S} becomes more positive and the output signal of the ASTEROID decreases. When



(a) Inversion: a too negative V_{CGoff} allows holes to flow also below the clear gate (CG) from drain (D) to source (S). Consequently, the output signal of the ASTEROID decreases.

(b) Injection: a too positive V_{CGoff} weakens the potential barrier between clear (C) and internal gate (iG), such that electrons are emitted from the clear (C) into the internal gate. Hence, the output signal of the ASTEROID increases.

Figure 4.5.10.: Schematic drawing of the inversion and injection mechanisms as well as the corresponding change in the output signal of the readout ASIC.

V_{CGoff} becomes too positive, see figure 4.5.10b, the potential barrier between clear contact and internal gate is weakened. Hence, electrons are emitted from the n-doped clear contact into the internal gate. The back emitted charge has the same effect as signal charge on the DEPFETs PMOS transistor. The transconductance of the channel is increased and thereby V_{S} decreases leading to an increase of the ASTEROID output signal. For strong injection V_{S} even leaves the input range of the ASTEROID.

In figure 4.5.11 (a) the output signal of the ASTEROID is displayed for the cut gate device operated with reference biasing and timing presented in section 4.3. The used time span includes the signal processing and multiplexing phases of row 61 to 64 and after the frame trigger row 1 to 4. When V_{CGoff} is shifted to more positive voltages, the potential barrier between internal gate and clear is lowered and eventually electrons are injected from the clear to the internal gate. This shows up on the oscilloscope as an increase of the ASTEROID output signal, see figure 4.5.11 (b). When V_{CGoff} becomes too negative, a parasitic transistor below the clear gate from drain to source is formed. It causes a decrease of the output signal in figure 4.5.11 (c). Injection as well as inversion do not start at exactly the same V_{CGoff} values for all pixels of the matrix due to the technological differences discussed earlier in section 3.3. The recognition of increased or decreased signal level for one of the pixels are the limits of the operation window for V_{CGoff}. The spectroscopic performance is stable within this operation window as will be shown in the following paragraphs.

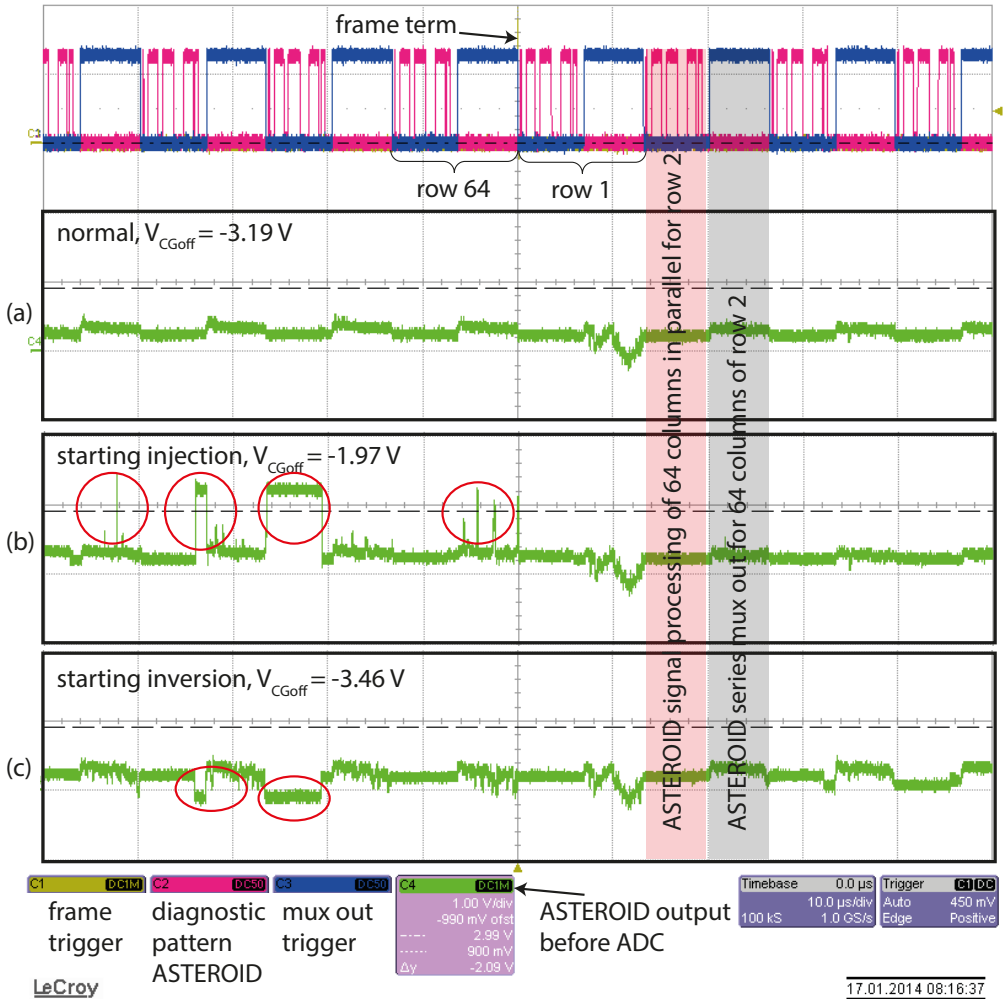
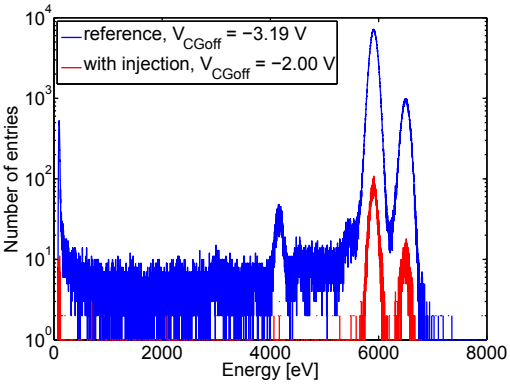
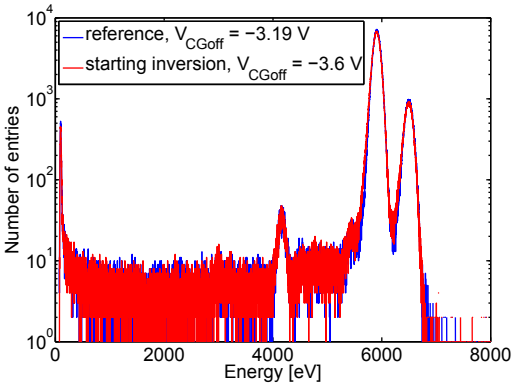


Figure 4.5.11.: (a) ASTEROID output signal (green) of the cut gate (CuG) detector for the reference or normal biasing from table 4.3.1 without radiation. When V_{CGoff} is (b) increased (more positive) or (c) decreased (more negative), the output signal changes because of injection or inversion respectively.

Leaving the operation window does not just cause a V_{S} shift but also a degradation of the measured spectrum. The histograms for all valid events of the injection and inversion points for the V_{CGoff} variation, which are indicated in figure 4.5.13b, are shown in figure 4.5.12. For injection bias conditions, the additional electrons in the internal gate lead to a significant loss of signal information as it is impossible to distinguish between signal electrons and injected electrons. In figure 4.5.12a the red spectrum measured under bias conditions at starting injection is compared to the blue reference spectrum. The histogram measured under bias conditions at starting inversion is shown in figure 4.5.12b in red. The drop of the current density in the PMOS transistor leads to a decrease of the internal amplification of the DEPFET. Thus, the noise contribution increases and the Mn-Kα_{1+2} peak broadens from $FWHM_{\mathrm{Meas}}$ of 135.6 eV to 137.2 eV.

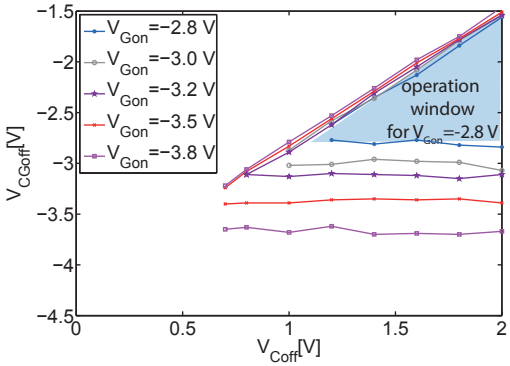


(a) Histogram of all valid events from the cut gate design for reference and injection bias conditions.

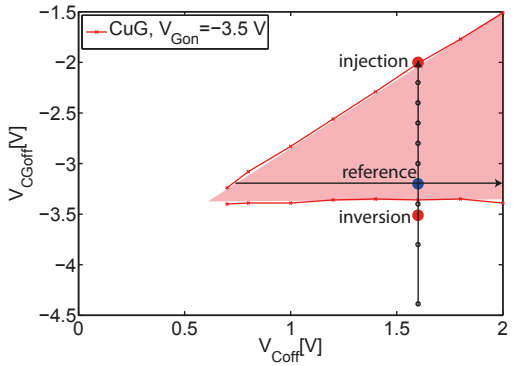


(b) All valid events spectra for reference and inversion bias conditions.

Figure 4.5.12.: The reference spectrum of the cut gate design measured using the biasing from table 4.3.1 is compared to the spectra of inversion and injection for V_{CGoff} indicated in figure 4.5.13b with red circles.



(a) V_{CGoff} operation window for the cut gate design for different V_{Gon} voltages.

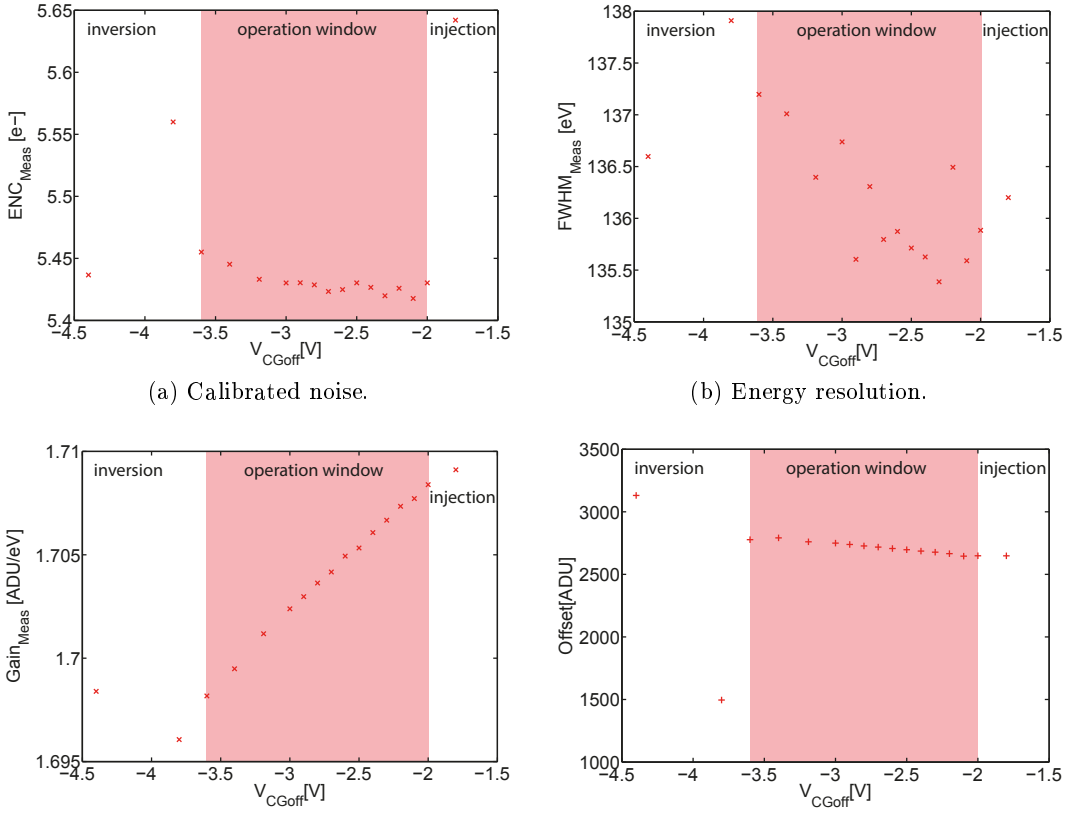


(b) V_{CGoff} operation window for V_{Gon}=-3.5 V with measurement series for V_{CGoff} variation (vertical line) and indicated V_{Coff} variation (horizontal line).

Figure 4.5.13.: The stable operation of the cut gate (CuG) detector is possible within the shaded areas. For more negative V_{CGoff}, inversion conditions start and for more positive V_{CGoff} or more negative V_{Coff}, charge from the clear contact is injected into the internal gate (iG).

The limits of the V_{CGoff} operation window are influenced by the applied gate on voltage V_{Gon} and the clear off voltage V_{Coff}. An array of operation windows for varied V_{Gon} and V_{Coff} are depicted in figure 4.5.13a for the cut gate DEPFET design. It can be seen that a more negative V_{Gon} as well as a more positive V_{Coff} broadens the operation window of V_{CGoff}. The cut gate devices can be operated properly in the area marked blue in figure 4.5.13a for a gate on voltage V_{Gon} of -2.8 V. With the

reference voltage V_{Gon} = -3.5 V from table 4.3.1, the operation window for V_{CGoff} estimated by using the oscilloscope is indicated in figure 4.5.13b by the red shaded area. Spectroscopic measurements are done across the range of clear gate off voltages indicated by the vertical line for the reference V_{Coff} voltage of 1.6 V.



(a) Calibrated noise.

(b) Energy resolution.

(c) System gain.

(d) Offset variation.

Figure 4.5.14.: Figures of merit for cut gate (CuG) design during V_{CGoff} variation. The absolute value of V_{CGoff} is given. The shaded area indicates the estimated operation window depicted in figure 4.5.13b.

In figure 4.5.14 the four figures of merit $FWHM_{\mathrm{Meas}}$, ENC_{Meas}, $Gain_{\mathrm{Meas}}$ and offset for the V_{CGoff} variation are presented for the cut gate design. The calibrated noise is similar for most of the measurement points and rises when the edges of the estimated operation window are reached. The energy resolution decreases, hence $FWHM_{\mathrm{Meas}}$ increases, for more negative V_{CGoff} as discussed for the histograms in figure 4.5.12. The gain decreases as well but on a smaller scale because the current density in the PMOS transistor gets lower and thus, the internal amplification decreases. The offset increases for more negative V_{CGoff}, has a minimum during establishing the parasitic transistor and rises again for the inversion measurement.

Within the operation window a stable detector performance is required in order to provide a reliable instrument performance. Thus, three criteria for the definition of the borders for stable detector operation have been specified in section 4.4.1. For the

variation of V_{CGoff}, the proper functionality of the DEPFET is not given anymore neither for V_{CGoff} values more positive than -2 V nor more negative than -3.6 V indicated by a significantly increased calibrated noise. Hence, the operation window estimated with the oscilloscope and the operation window defined by the spectroscopic measurements match for this measurement series.

In figure 4.5.14 a measurement point in deep inversion for V_{Goff} = -4.4 V is shown. The cut gate detector shows stable performance at this point but with a significant current flowing from the DEPFET's PMOS to the backside contact. This is unwanted and thus, the measurement point is not considered as part of the stable operation window. A measurement for a fully established parasitic transistor in deep inversion, see figure 4.5.10a, is only possible for the cut gate design. For all other designs the clear gate is directly connected to the drain. That means for an inversion bias of V_{CGoff} the parasitic transistor cannot be switched off by the gate. Thus, there is a parasitic current in the whole matrix at all times independent of the on or off-state of the pixels.

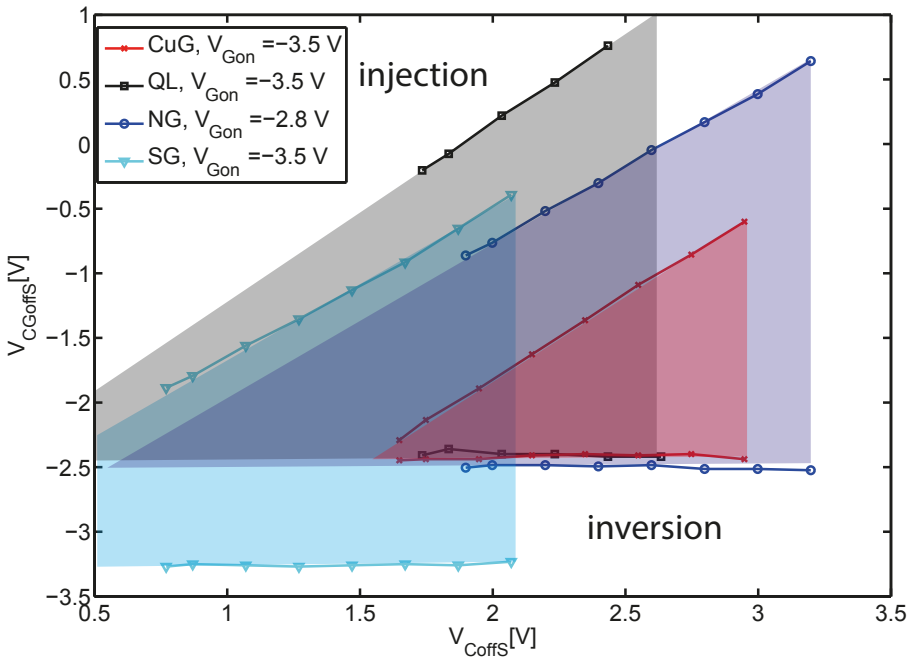


Figure 4.5.15.: Estimated operation windows of the clear gate V_{CGoff} and clear V_{Coff} bias referred to source potential V_{S} for all DEPFET design variants: CuG = Cut Gate, QL = Quasi Linear, NG = Narrow Gate, SG = Short Gate.

In order to compare the different DEPFET designs, the shifted voltage V_{CGoff} is referred to the source potential V_{S} and written as V_{CGoffS}. This is done for all voltages in the following and the appendix sections where the designs need to be compared. The referring does not change the curve shape but shifts it and allows to compare the designs within the same frame of reference. The operation windows estimated with the oscilloscope for V_{CGoffS} and V_{CoffS} for the DEPFET designs are shown in figure 4.5.15. As gate on voltage V_{Gon} the reference points from table 4.3.1 are used.

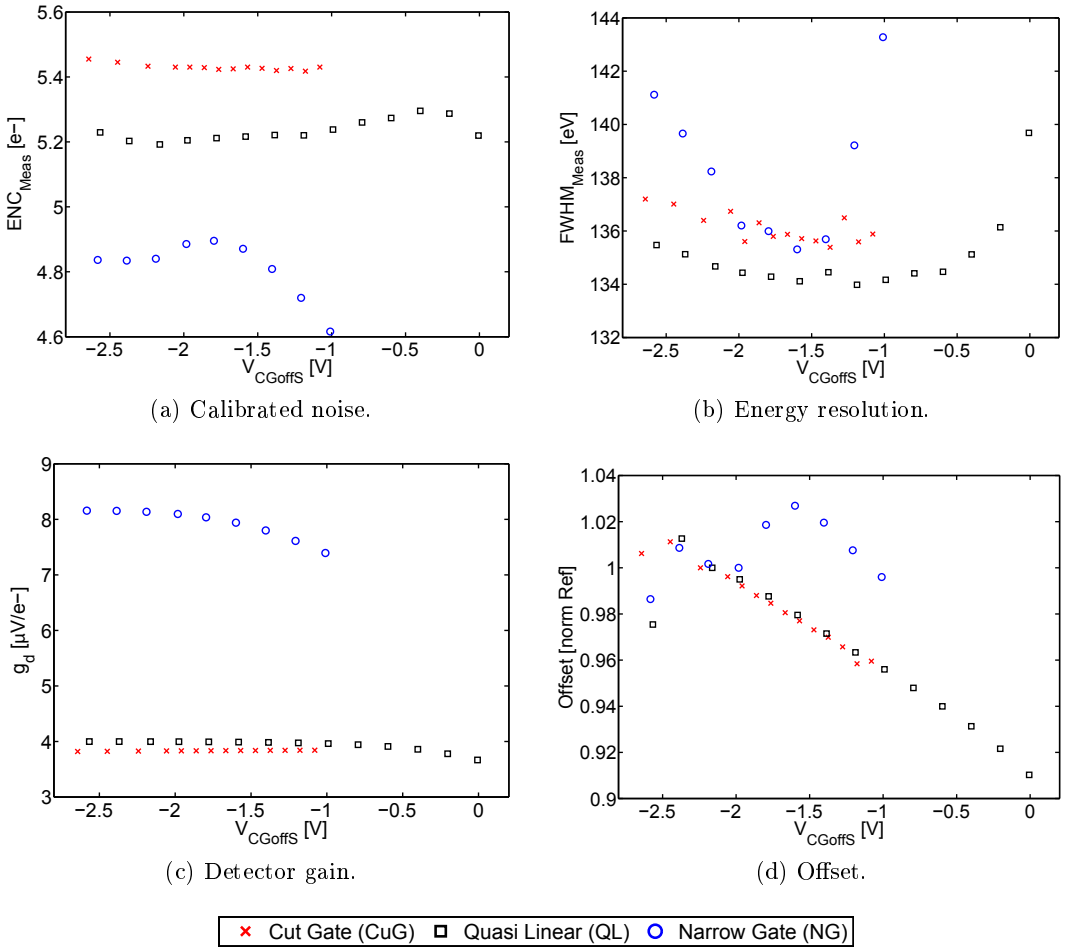
The short gate design is shown also because the determination using the oscilloscope described above can be done for the short gate despite of the potential pocket and the charge loss.

The shaded areas of stable operation are not elongated towards more positive V_{CoffS} because when they reach V_{Conset} discussed in section 3.3.4, the clear can drain electrons from the internal gate and deteriorate the energy resolution. The increase of $FWHM_{\mathrm{Meas}}$ was endorsed by the V_{CoffS} variation and is shown in the appendix in figure A.2.1. For a fixed V_{CoffS}, e.g. +2 V, the four designs allow different shifts of V_{CGoffS} for proper operation. The quasi linear device can cope with a V_{CGoff} variation of 2.6 V, the narrow gate design with 1.8 V and the cut gate with about 0.5 V. From the oscilloscope analysis the quasi linear design has the widest operation range and the well known default, the cut gate, the smallest for the chosen reference point. A wide operation window is preferred for Athena because the window shrinks with increasing radiation damage. As known from figure 4.5.13, the gate on potential V_{Gon} influences the position and width of the window and so do several other voltages. This emphasizes that the DEPFET biasing is a multi-dimensional space with parameters influencing each other. That is why a fixed reference point is defined for each design and starting there only one parameter at a time is varied.

Excluding the short gate design because of its poor detector performance, the V_{CoffS} of the reference points are between +2.2 V and +2.5 V for the V_{CGoffS} variation. The figures of merit within the operation windows are illustrated in figure 4.5.16 for the three designs. The ranges of stable detector operation have been defined for the quasi linear and narrow gate design variants using the three criteria from section 4.4.1 as described above for the cut gate design. In addition to figure 4.5.16, the measurement range, operation window and the variation of the figures of merit are summarized in table 4.5.5.

The operation window for the V_{CGoff} variation is restricted by the functionality of the DEPFET. For the cut gate design this was indicated by a suddenly increased measurement noise as shown in figure 4.5.14. For the quasi linear as well as the narrow gate design, the energy resolution $FWHM_{\mathrm{Meas}}$ shows a parabolic shape that increases in direction of inversion and injection. Thus, the operation window of those two designs is restricted firstly by $FWHM_{\mathrm{Meas}}$ increasing above 150 eV. It is supposed that the parabolic curve shape depends on the capacitive coupling between gate and clear gate, which increases with the overlapping area between those polysilicon structures. All in all the quasi linear design has the largest operation window $\Delta V_{\mathrm{CGoff}} = 2.6$ V for the chosen reference voltages of table 4.3.1.

By comparing the most positive V_{CGoffS} for the operation windows in table 4.5.5 to the clear gate onset voltage V_{CGonset} measured with the quasi-static electrical setup and taken from table 3.3.12, clearly V_{CGoffS} is always more negative than V_{CGonset}. This shows that the quasi-static electrical characterization of the clear structure predicts the dynamic operational parameter. The difference between the mean prediction and the applied detector bias is due to the deviation of V_{CGonset} within one matrix, which is larger for the narrow gate design than for cut gate or quasi linear



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

(d) Offset.

Figure 4.5.16.: Figures of merit within the operation window for all designs for V_{CGoff} variation. For the comparison the V_{CGoff} voltage is referred to the source potential and given as V_{CGoffS}.

structures.

The cut gate design shows the highest noise of 5.5 e^- and the narrow gate the lowest with about 4.7 e^-. This correlates inversely with the DEPFET gain g_{d}, that is a measure of the signal amplification of the DEPFET. It is defined by equation 2.2.34 as the relation of charge transconductance g_{q} to transconductance g_{m}. In section 3.3.2 has been derived from the quasi-static electrical qualification measurements that the narrow gate design has the highest g_{m}. It shows also the highest g_{d} for the dynamic spectroscopic measurements. This leads to the conclusion, that g_{q} must be two times higher than those of cut gate and quasi linear design. It is supposed that the collected signal electrons in the internal gate have a greater impact on the transistor transconductance owing to the higher current density in the channel resulting from the smaller gate dimensions at an equal total current I_{PMOS}. A discussion of this topic can be found in section 4.5.4. Nevertheless, a two times higher g_{d} does not lead to half ENC_{Meas}. For a significant higher g_{d} a lower amplification mode of the

	Cut Gate	Quasi Linear	Narrow Gate
measurement range V_{CGoff} [V]	-4.40↗-1.80	-3.60↗-0.40	-3.80↗-1.6
injection starts @ V_{CGoff} [V]	-2.00	-1.00	-2.20
inversion starts @ V_{CGoff} [V]	-3.60	-3.60	-3.80
operation window V_{CGoff} [V]	-3.60↗-2.00	-3.60↗-1.00	-3.80↗-2.20
operation window V_{CGoffS} [V]	-2.64↗-1.08	-2.57↗0.01	-2.58↗-1.01
mean $V_{CGonset}$ $[V]$	-0.92	+0.02	-0.68
ENC_{Meas} [e^-]	5.42↗5.46	5.19↗5.30	4.62↗4.90
$FWHM_{\mathrm{Meas}}$ [eV]	135.4↗137.2	134↗139.7	135.3↗143.3
Offset [norm. Ref]	0.96↗1.01	0.91↗1.01	0.99↗1.03
g_{d} [µV/ e^-]	3.82↗3.84	3.67↗4.00	7.39↗8.16
operation window $\Delta V_{\mathrm{CGoff}}$ [V]	1.60	2.60	1.60
$\Delta ENC_{\mathrm{Meas}}$ [e^-]	0.04	0.10	0.28
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	1.81	5.70	7.97
ΔOffset [norm. Ref]	0.05	0.10	0.04
Δg_{d} [µV/ e^-]	0.02	0.33	0.76

Table 4.5.5.: Measurement range and operation window for V_{CGoff} for the DEPFET designs defined after the criteria from section 4.4.1. Δ equals the difference between highest and lowest measured value within the operation window.

ASTEROID readout ASIC must be used in order to stay in the ADC input range. The different setting of the readout ASIC changes ENC_{Filter} and thus ENC_{Meas}.

The offset depicted in figure 4.5.16d decreases for more positive V_{CGoffS}. The more positive the clear gate off voltage, the higher the chance that leakage current accumulates not exclusively in the internal gate but also underneath the clear gate. This leads to a gradual decreasing offset. The offset is normalized to the reference point offset for all designs for comparability.

The analysis of the measurement series for all other voltage variations is done in the same way as described here for V_{CGoff}. The detailed discussion of all results is beyond the scope of this chapter. For completeness, the other measurement series are presented in the appendix starting at A.2.1. A comparative valuation of the operation windows for the different designs is given in section 4.6.

Constant source potential

For the measurement series discussed in the last section and in the appendix, the source potential V_{S} shifts with the varied biasing parameter. The source follower readout mode used here keeps the transistor current I_{PMOS} constant using a current source and measures the modulation of the channel conductivity by means of the V_{S} shift. The source potential V_{S} is the free parameter for the DEPFET that adjusts to

any given change of the biasing as explained in section 4.3.2. This leads to a shift of the frame of reference for all applied voltages of the DEPFET during a measurement series. It is possible to keep the source potential V_S constant by adjusting it with the gate voltage V_G. The difference between a floating and constant source potential within a parameter variation is examined in the following paragraphs for the transistor current I_{PMOS} measurement series.

The transistor current I_{PMOS} is modified using the current source of the ASTEROID for the source follower readout. As a result of the changed I_{PMOS}, the source potential V_S shifts because the drain potential V_D as well as the gate on potential V_{Gon} are fixed. According to equation 2.2.18 the PMOS transistor current in the saturation region is defined by

$$I_{PMOS} = -\frac{\beta}{2}(V_{GS} - V_{Th})^2 \cdot (1 - \lambda V_{DS})$$

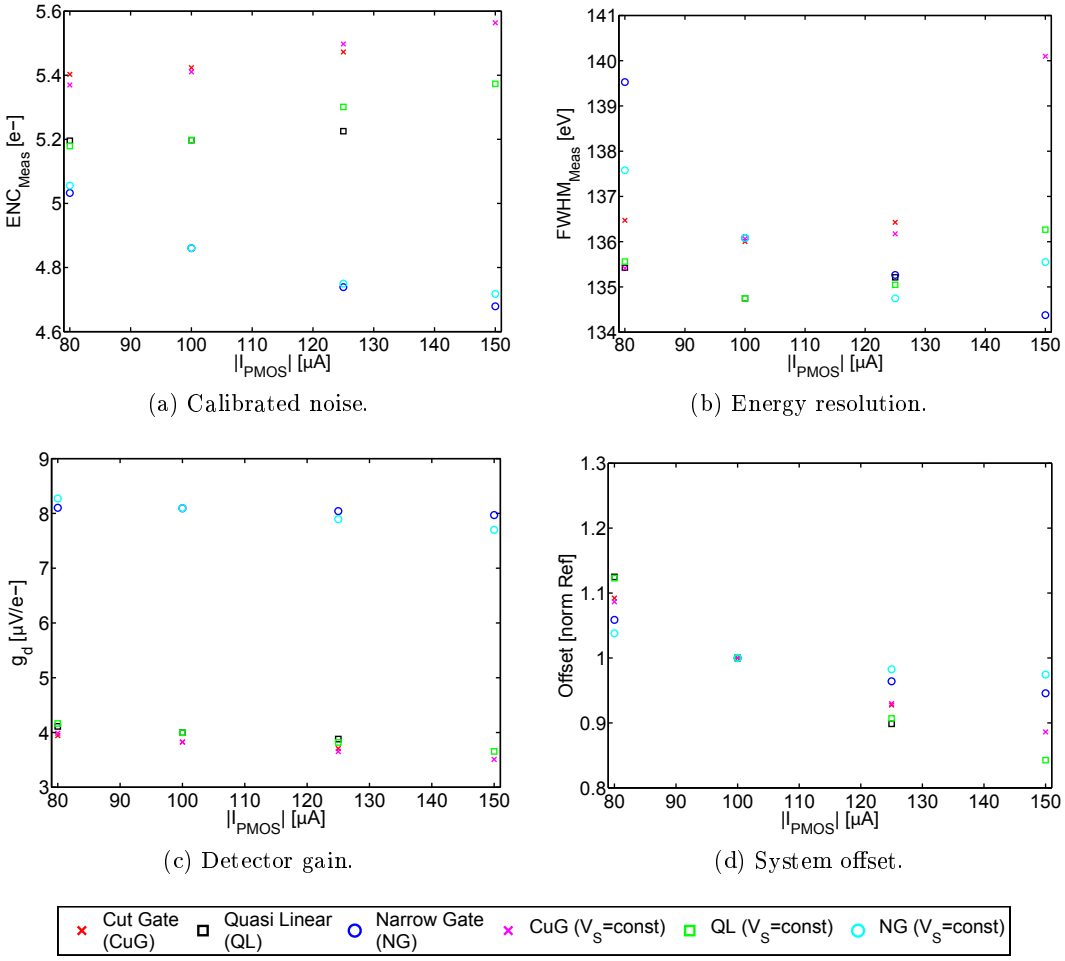
When V_S is shifted, also V_{GS} and V_{DS} are changed and not to mention V_{CoffS}, V_{ConS} and V_{CGoffS}. If the source potential V_S is kept constant by adjusting the gate bias V_{Gon}, only V_{GS} will change in the equation but neither V_{DS} nor the NMOS biasing.

In order to compare the measurement series with and without constant source potential, the limits of the operation window from $I_{PMOS}(V_S \neq \text{const.})$ are also applied to $I_{PMOS}(V_S = \text{const.})$. Thus, the current $|I_{PMOS}|$ is varied between 80 µA and 150 µA. For lower currents the source potential becomes too negative for the ASTEROID input range. For higher currents leading to more positive V_S and thus to more positive V_{GonS}, the operation window for V_{CGoffS} is left. Only for the narrow gate design a measurement for $|I_{PMOS}| = 150$ µA is possible with varying V_S. For the cut gate and quasi linear device, V_{CGoffS} with -2.7 V for this measurement point lies outside the operation window, see figure 4.5.15. The results for the figures of merit of the three DEPFET designs are compared in figure 4.5.17. The parameter for the measurement series are summarized in tables 4.5.6 and 4.5.7 respectively.

The first distinctive feature in figure 4.5.17 is that the shape of the parameter function is similar for varied and constant V_S within each design. Secondly, the ENC_{Meas} in figure 4.5.17a increases with increasing transistor current for the cut gate and the quasi linear DEPFET. This was expected because of a rise of the thermal noise in equation 2.2.35 of ENC_{Filter} for higher currents. In contrast to cut gate and quasi linear structures, the narrow gate device has an decreasing equivalent noise charge ENC_{Meas} for an increasing transistor current I_{PMOS}. This is also in contrast to the slightly decreasing detector gain g_d depicted in figure 4.5.17c. In section A.2.1 it has been derived that

$$ENC_{Filter} \propto C_{Det} \propto \frac{1}{g_d}$$

Thus, an increase of the equivalent noise charge would be expected. The distinction of the narrow gate design needs to be investigated by 3D simulations as its behavior could not be explained by transistor or noise theory. The increased noise prevents an improvement of the energy resolution meaning the $FWHM_{Meas}$ does not decrease with increasing I_{PMOS}.



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

(d) System offset.

Figure 4.5.17.: Comparison between the figures of merit for I_{PMOS} variation and $I_{\mathrm{PMOS}}(V_{\mathrm{S}} = \mathrm{const.})$ variation.

According to equation 2.2.34, the gain is defined as

$$g_{\mathrm{d}} = \frac{g_{\mathrm{q}}}{g_{\mathrm{m}}}$$

When during the derivation of g_{m} and g_{q} from the transistor current formula 2.2.30, the substitution

$$\left(\frac{f \cdot Q_{\mathrm{iG}}}{C_{\mathrm{G}}} + V_{\mathrm{GS}} - V_{\mathrm{Th}}\right) = \sqrt{-\frac{I_{\mathrm{PMOS}} \cdot 2}{\beta}}$$

is performed, g_{m} becomes

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{PMOS}}}{\partial V_{\mathrm{GS}}} = -\sqrt{\beta \cdot (1 - \lambda \cdot V_{\mathrm{DS}})} \cdot \sqrt{-2 \cdot I_{\mathrm{PMOS}}} \tag{4.5.2}$$

and g_{q}

$$g_{\mathrm{q}} = \frac{\partial I_{\mathrm{PMOS}}}{\partial Q_{\mathrm{iG}}} = -\sqrt{\frac{\beta \cdot f^2 \cdot (1 - \lambda \cdot V_{\mathrm{DS}})}{C_{\mathrm{G}}^2}} \cdot \sqrt{-2 \cdot I_{\mathrm{PMOS}}} \tag{4.5.3}$$

	Cut Gate	Quasi Linear	Narrow Gate
measurement range/ operation window $\lvert I_{\mathrm{PMOS}}\rvert$ [µA]	80↗125	80↗125	80↗150
ENC_{Meas} [e^-]	5.40↗5.47	5.20↗5.23	4.68↗5.03
$FWHM_{\mathrm{Meas}}$ [eV]	136.0↗136.5	134.8↗135.4	134.4↗1.39.53
Offset [norm. Ref]	0.93↗1.09	0.90↗1.12	0.95↗1.06
g_{d} [µV/ e^-]	3.71↗3.94	3.88↗4.11	7.97↗8.10
operation window ΔI_{PMOS} [µA]	45	45	45
$\Delta ENC_{\mathrm{Meas}}$ [e^-]	0.07	0.03	0.35
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	0.5	0.7	5.2
ΔOffset [norm. Ref]	0.16	0.23	0.11
Δg_{d} [µV/ e^-]	0.24	0.23	0.13

Table 4.5.6.: Results of the I_{PMOS} variation. Δ equals the difference between highest and lowest measured value within the operation window.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range/ operation window $\lvert I_{\mathrm{PMOS}}\rvert$ (V_{S} =const.) [µA]	80↗150	80↗150	80↗150
ENC_{Meas} [e^-]	5.37↗5.56	5.18↗5.37	4.72↗5.06
$FWHM_{\mathrm{Meas}}$ [eV]	135.4↗140.1	134.8↗136.3	134.8↗137.6
Offset [norm. Ref]	0.89↗1.09	0.84↗1.12	0.97↗1.04
g_{d} [µV/ e^-]	3.51↗3.99	3.66↗4.16	7.70↗8.27
operation window $\Delta\lvert I_{\mathrm{PMOS}}\rvert$ (V_{S} =const.) [µA]	70	70	70
$\Delta ENC_{\mathrm{Meas}}$ [e^-]	0.19	0.19	0.34
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	4.7	1.5	2.8
ΔOffset [norm. Ref]	0.20	0.28	0.06
Δg_{d} [µV/ e^-]	0.48	0.51	0.57

Table 4.5.7.: Results of I_{PMOS} variation with constant source potential V_{S}. Δ equals the difference between highest and lowest measured value within the operation window.

These equations show that g_{d} in theory should be constant because g_{m} and g_{q} would increase equal for increasing I_{PMOS}. As g_{d} decreases, it points towards that g_{m} raises more than g_{q}. In addition, figure 4.5.17c shows that the decrease of g_{d} is more dominant for the measurement series with constant source potential V_{S}. For a varying source potential, V_{S} gets more positive for an increasing transistor current I_{PMOS}. This leads to an increase of the potential drop between source and drain V_{DS} that actually leads to an increase of g_{d} as shown in section A.2.1. These effects compensate each other partially. All in all, the behavior is similar for varying and constant source potential but the operation window has been increased by fixing V_{S}.

Operation timing

Besides the applied voltages also the timing of the measurement sequence from section 4.3.1 has been varied. The goal of the timing measurements is to find the shortest timing possible, which still shows the full detector performance in order to maximize the readout speed and the throughput. For the readout sequence shown in figure 4.3.1, three timings in addition to the whole frame time t_{Frame} presented in section 4.5.1 have been varied:

- clear time t_{Clear}: duration of the clear process meaning clear and clear gate are in their on-state in order to remove the electrons from the internal gate. The reference t_{Clear} used for spectroscopic measurements is 700 ns.

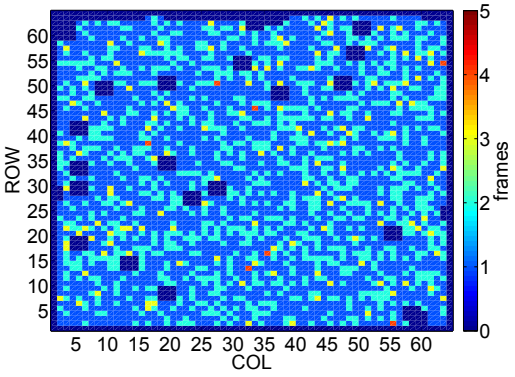
- settling time t_{Settle}: delay after the clear process before the second readout phase with t_{Read} starts to ensure a stable baseline for the second sample. For the reference sequence t_{Settle} is 1350 ns.

- overlap time between the clear and clear gate off-state t_{Overlap}: time gap between the switching of the clear gate from on to off-state and the switching of the clear to off-state in order to prevent back injection. The reference for t_{Overlap} is 50 ns.

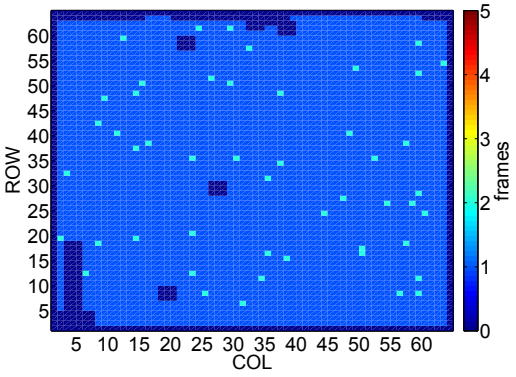
As explained in section 4.3.1, if either t_{Clear} or t_{Settle} are shortened, the other time will be extended. Thus, t_{Frame} stays constant. This is done in order to minimize the influence of an increasing leakage current on the detector performance close to the speed limit. t_{Clear}, t_{Overlap} and t_{Settle} are increased by adding clock cycles, which leads to an increase of the total frame time t_{Frame}. Nevertheless, extending t_{Clear}, t_{Overlap} and t_{Settle} is not expected to have an impact on the detector performance. Hence, an increase of leakage current is tolerated.

As mentioned before, t_{Clear} is the time for the actual removal of the signal charge from the internal gate. That means for a too short clear time, signal electrons remain in the internal gate and the pixel is marked wrongly as hit by a photon again in the following frame. Thus, the parameter indicating the minimal t_{Clear} is the so-called clear correlation. The clear correlation shows the maximum of sequenced frames in which a pixel, which has been hit by a photon once, is marked as hit. The clear correlation map for the cut gate device is displayed in figure 4.5.18a for $t_{\mathrm{Clear}} = 200$ ns and in figure 4.5.18b for $t_{\mathrm{Clear}} = 1400$ ns. For the short t_{Clear} most pixel appear as hit over two and more frames. This shows that 200 ns are too short for a complete clear process under the given measurement conditions. Ideally most pixel show up in average only once after an event like for a clear time of 1400 ns in figure 4.5.18b. The minimum t_{Clear} is chosen such, that the average maximum clear correlation length is below 1.05 frames meaning that less than 5% of the pixels are marked in more than one frame as hit for one photon. The minimum t_{Clear} is presented in table 4.5.8.

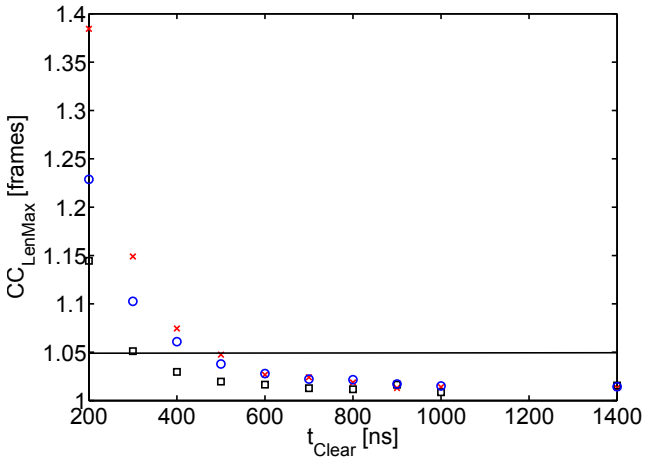
The clear correlation length of the quasi linear design drops below the limit of 1.05 frames for $t_{\mathrm{Clear}} = 400$ ns. The cut gate and narrow gate design follow at $t_{\mathrm{Clear}} = 500$ ns. This indicates that either the potential connection between the internal gate and the clear contact is established quicker or that the drift velocity of the signal



(a) Clear correlation map of the cut gate design for cleartime $t_{\mathrm{Clear}} = 200$ ns.



(b) Clear correlation map of the cut gate design for cleartime $t_{\mathrm{Clear}} = 1400$ ns.



(c) The limit of the average maximum clear correlation length is chosen as 1.05 frames per device.

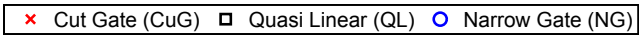
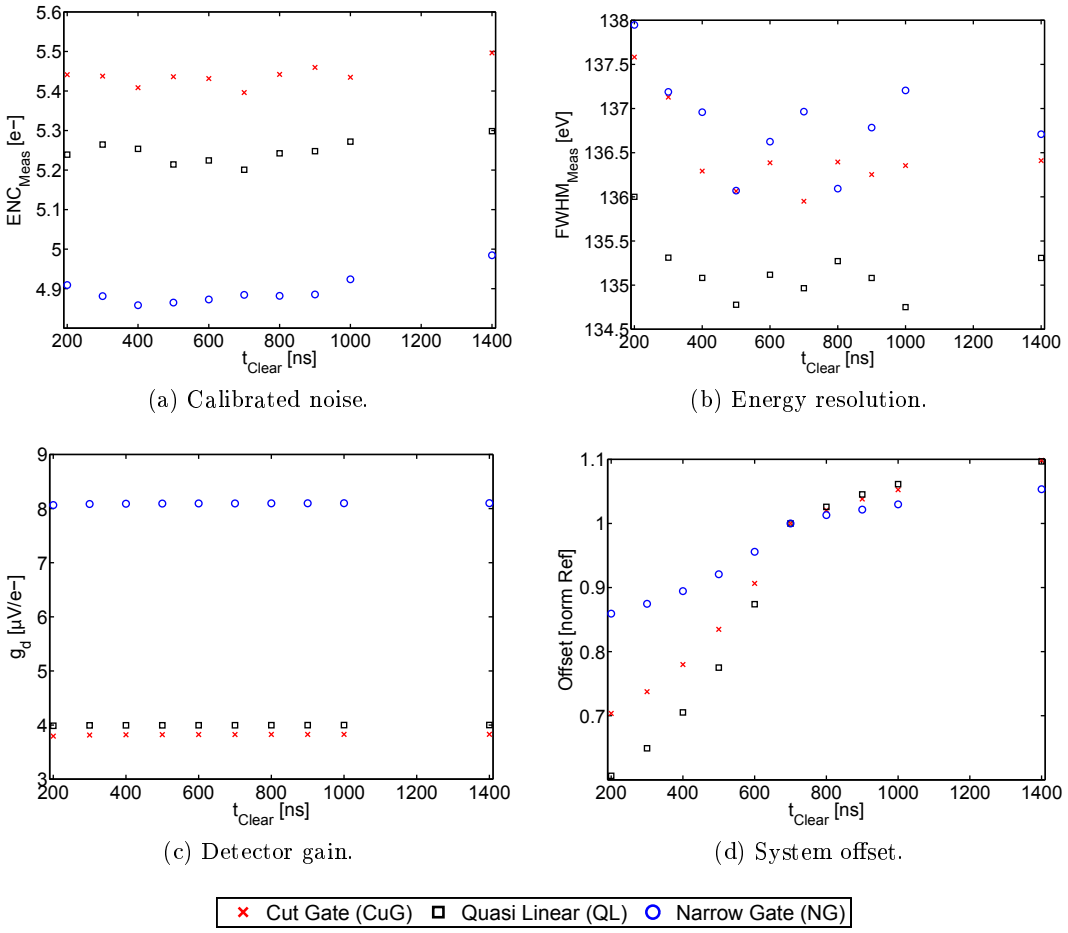


Figure 4.5.18.: The clear correlation shows the maximum of sequenced frames in which a pixel, which has been hit by a photon once, is marked as hit. If the clear functions properly, an event will be recognized ideally only in one frame.

electrons is higher for the quasi linear design. Also a combination of the two explanations is possible. The cut gate design shows in figure 4.5.18c for all $t_{\mathrm{Clear}} < 800$ ns the longest clear correlation length within the DEPFET designs.

The figures of merit used throughout the voltage variations are depicted in figure 4.5.19 for the t_{Clear} measurement series. It can be seen that the varied clear time t_{Clear} has no systematic influence on these parameters despite of the system offset. This results from the data analysis software ROAn, which has been presented in section 4.4.2. ROAn does not only mark pixel clusters after split events, it also marks time clusters like the clear correlations. Hence, the hit pixel is respected only once per event for further calculations of e.g. the energy resolution. The system offset decreases with shorter t_{Clear} because the settling time t_{Settle} after the clear process



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

(d) System offset.

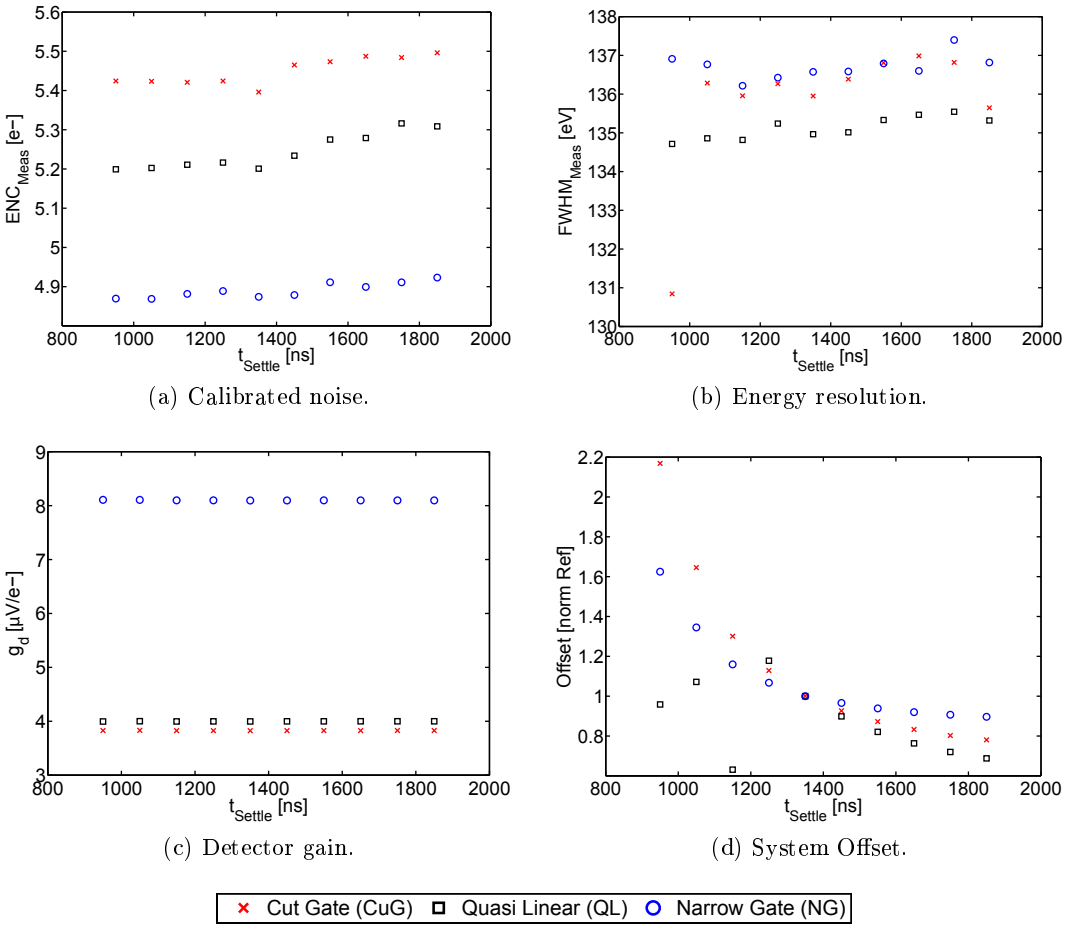
Figure 4.5.19.: The four figures of merit are plotted versus the varied clear time t_{Clear} for the three DEPFET designs.

is elongated, see again figure 4.3.1, as the row time t_{Row} and frame time t_{Frame} are kept constant. The slight increase of the offset for $t_{\mathrm{Clear}} > 700$ ns is caused by the increased t_{Frame}. As expected, a further increase of the clear time has no effect on the figures of merit and works against the required throughput for Athena.

In addition to the total clear time also the overlap between the clear and clear gate on-state t_{Overlap} has been varied. In order to prevent back injection from the clear into the internal gate, t_{Overlap} is necessary as discussed in section 2.2.3. For all measurements the general clock of the X-Board was set to a frequency of 20 MHz. Hence, the minimum change in the timing is one clock cycle of 50 ns. It was found, that an overlap time $t_{\mathrm{Overlap}} = 50$ ns is sufficient and a further increase has no impact on the detector performance, see table 4.5.8. Without overlap time, no spectrum could be measured at all.

The DEPFET source and the ASTEROID input together form a RC-circuit that needs a certain time t_{Settle} after the clear process to reach its baseline. When t_{Settle} is too short, the baseline sampling is done within the falling edge, which leads to an

increase of the pixel offset. Thus, one limitation for the t_{Settle} measurement series is the input range of the ADC in the measurement setup. As for the clear time variation, the elongation of the settling time is expected to not improve the spectroscopic performance. The figures of merit for the t_{Settle} variation are displayed in figure 4.5.20.



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

(d) System Offset.

Figure 4.5.20.: Comparison of the figures of merit for the settling time t_{Settle} variation between the DEPFET designs.

For too short settling times, the input range of the ADC is exceeded by the output signal of the ASTEROID. Hence, the calibration peaks are not recorded completely. The effect is visible for $t_{\mathrm{Settle}} = 950$ ns of the cut gate design in the energy resolution $FWHM_{\mathrm{Meas}}$ in figure 4.5.20b. The Mn-Kα_{1+2} peak is only partially recorded leading to an under estimation of $FWHM_{\mathrm{Meas}}$. Therewith, the cut gate design requires with $t_{\mathrm{Settle}} = 1050$ ns a longer settling time than quasi linear and narrow gate structures. This indicates, that the cut gate design has the highest input capacitance of the three designs. Note, that the calibrated noise ENC_{Meas} and as a result $FWHM_{\mathrm{Meas}}$ increase slightly due to the elongation of the total frame time for $t_{\mathrm{Settle}} > 1450$ ns. Despite of the offset, the settling time shows no influence on the figures of merit. The operation minimum for t_{Settle} is given in table 4.5.8.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range t_{Overlap} [ns]	0↗150	0↗150	0↗150
operation minimum [ns]	50	50	50
measurement range t_{Clear} [ns]	200↗1400	200↗1400	200↗1400
operation minimum [ns]	500	400	500
measurement range t_{Settle} [ns]	950↗1850	950↗1850	950↗1850
operation minimum [ns]	1050	950	950

Table 4.5.8.: Results of the timing variations: The arrow illustrates the direction of the time variation. The operation minimum is the fastest timing possible in order to ensure proper clear performance and detector settling.

When for all varied timing parameter the operation minimum is used, a speed increase of 4% compared to the reference timing can be achieved. This is clearly not sufficient to increase the throughput of the detector noticeable. The readout time for one row t_{Row} can be halved by reading one row and multiplexing the previous row in parallel resulting in $t_{\mathrm{Row}} = 5.2$ µs instead of 13.25 µs as done for the DEPFET detector of the MIXS instrument [9]. The row readout time can be further decreased by increasing the general timing clock frequency of the setup to 26.7 MHz. Thus, the multiplexing time is shortened by one third. Increasing the frequency further is not possible with the ASTEROID, as the clock frequency of its digital part is limited.

Summarizing it can be said, that the required $t_{\mathrm{Row}} = 2$ µs for Athena [7] cannot be reached with the current source follower readout. Instead the drain readout is the preferred solution because it does not require a settling time t_{Settle}.

4.5.4. Reference to electrical qualification measurements

So far, the spectral resolution, the width of the operation windows as well as the noise of the DEPFET design variants have been investigated. The measured gain $Gain_{\mathrm{Meas}}$ was an essential parameter for the assessment of a measurement series. $Gain_{\mathrm{Meas}}$ implies all conversion and amplification phases within the detector as shown as schematic drawing in figure 4.5.21.

When a photon is absorbed in the bulk of the DEPFET, it generates electron-hole pairs, see section 2.1 for a detailed discussion. The signal electrons are collected in the internal gate and are converted to a source potential shift of the DEPFET as stated in section 2.2.3 for the source follower readout. The conversion constant is the so-called detector gain g_{d}, which is used as figure of merit throughout the comparison of the spectroscopic performance between the DEPFET variants, see section 4.5.3. Finally, the potential shift is converted and amplified by the ASTEROID and the detector periphery to a digital signal that can be stored and analyzed.

With the spectroscopic measurement setup, the internal amplification of the DEPFET, also referred to as charge transconductance g_{q}, cannot be measured directly. Thus,

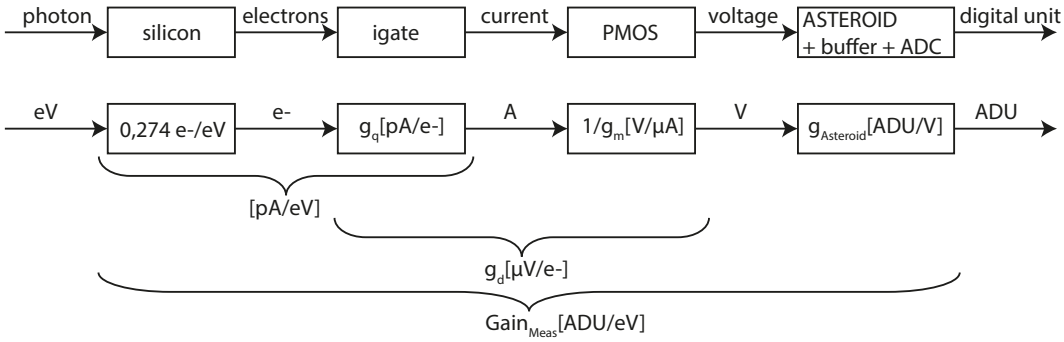


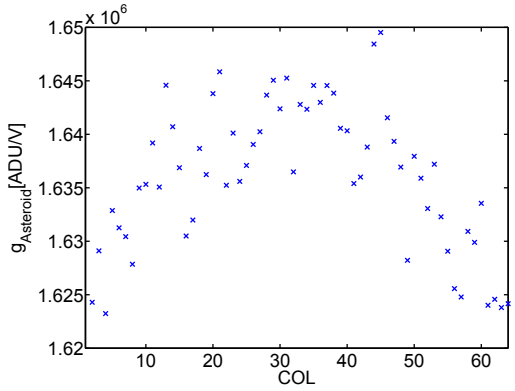
Figure 4.5.21.: Schematic drawing of the conversion and amplification phases within the DEPFET detector from the absorbed photon to the digital signal information for the source follower readout.

the combination of the electrical qualification and spectroscopic measurements reveals the behavior of the charge transconductance. In the source follower configuration, the source potential adjusts to every biasing voltage change but the electrical qualification has been done for a fixed V_{S}. Hence, just the determination of g_{q} for the I_{PMOS} variation with fixed source potential, which is presented in section 4.5.3, is the most appropriate.

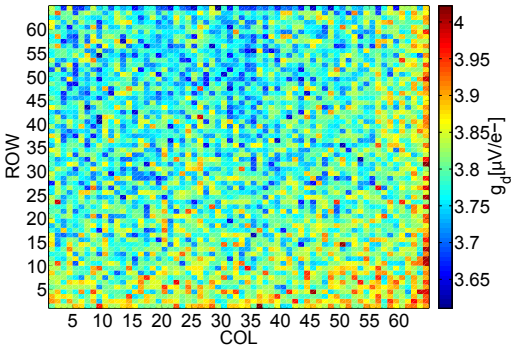
The steps of the determination of the charge transconductance g_{q} are illustrated by figure 4.5.22 for the cut gate device F20 of wafer 35. Starting point is the gain map $Gain_{\mathrm{Meas}}$ depicted in figure 4.4.1c. $Gain_{\mathrm{Meas}}$ comprises the column-wise amplification of the setup periphery and readout ASIC g_{Asteroid}, the PMOS transconductance g_{m} as well as the charge transconductance g_{q}. g_{Asteroid} was measured for all detector hybrids with the spectroscopic setup before the DEPFET devices have been populated. It is shown in figure 4.5.22a for the detector hybrid of device F20 of wafer 35. $Gain_{\mathrm{Meas}}$ of each pixel is divided by the corresponding channel gain g_{Asteroid} resulting in the detector gain g_{d}, which can be seen in figure 4.5.22b. The detector gain is the ratio of g_{q} to g_{m}. The transconductance g_{m} was determined for the pixel-wise transfer characteristics as the slope at V_{On}, see figure 4.5.22c. The evaluation of g_{m} has been discussed in section 3.3.2. As the reference transistor current $|I_{\mathrm{PMOS}}|$ is 100 µA for the spectroscopic measurement series, g_{d} for each pixel is multiplied by the corresponding transconductance value g_{m}. The charge transconductance g_{q} thus gained is depicted in figure 4.5.22d.

The measurement series of $|I_{\mathrm{PMOS}}|$ ranges from 80 µA to 150 µA. In order to calculate g_{q} for every measurement point, the transconductance g_{m} was determined as slope of the transfer characteristics for the different transistor currents and is shown in figure 4.5.23a. In figure 4.5.23b the detector gain of this measurement series is depicted. The course of g_{q} versus I_{PMOS} for the three DEPFET designs, which results from multiplying g_{d} with g_{m} for each pixel of a matrix, is displayed in figure 4.5.23c. Additionally, the values of g_{m}, g_{d} and g_{q} for the measurement point $|I_{\mathrm{PMOS}}| = 100$ µA are summarized in table 4.5.9.

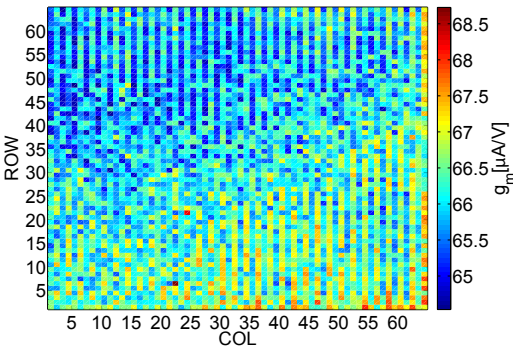
The charge transconductance increases for an increasing transistor current for all



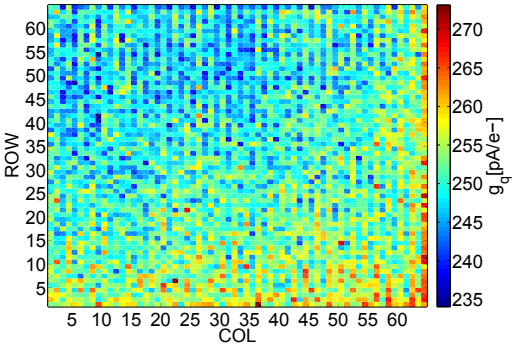
(a) Amplification of the readout ASIC and the used measurement setup.



(b) Detector gain.



(c) Transconductance.



(d) Charge transconductance.

Figure 4.5.22.: Maps of the conversion and amplification parameters for the cut gate (CuG) device F20 of wafer 35 with reference bias.

	Cut Gate	Quasi Linear	Narrow Gate
g_m [μ A/V]	66	63	74
g_q [pA/ e^-]	239	250	594
$g_\mathrm{q}/g_\mathrm{m}$ [μ V/ e^-]	3.62	3.97	8.03

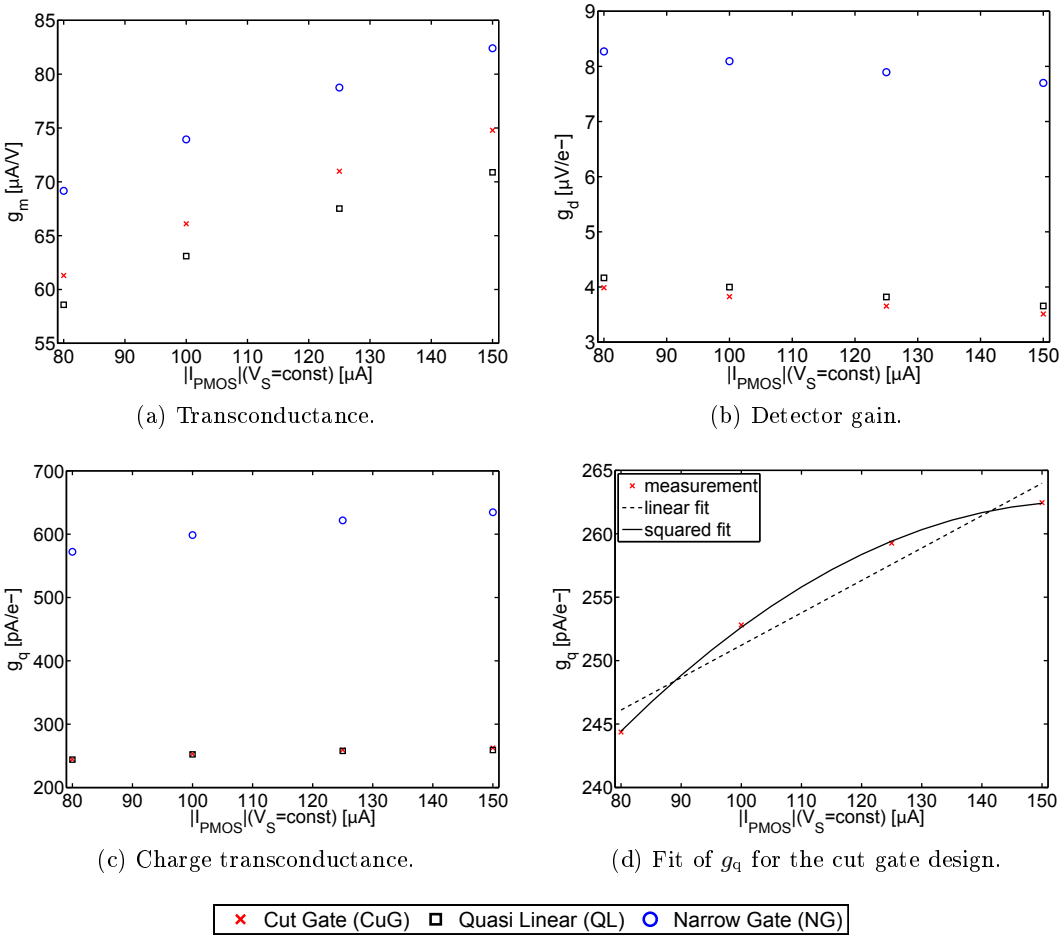
Table 4.5.9.: The interrelation between gain g_d, transconductance g_m and charge transconductance g_q are presented for the reference bias $|I_\mathrm{PMOS}| = 100$ µA of the DEPFET designs.

DEPFET variants. This has been expected because the impact from the signal charge onto the channel conductivity must be more effective for higher current densities. A close up on the curve shape of g_q is displayed in figure 4.5.23d for the cut gate device. As derived before in equation 4.5.3, g_q is expected to depend on I_PMOS as

$$g_\mathrm{q} \propto \sqrt{-2 \cdot I_\mathrm{PMOS}}$$

but a fit using a square root equation is not constructive for g_q versus I_PMOS. Instead a linear dependency with

$$g_\mathrm{q}(I_\mathrm{PMOS}) = 0.2554 \cdot I_\mathrm{PMOS} + 225.7$$



(a) Transconductance.

(b) Detector gain.

(c) Charge transconductance.

(d) Fit of g_q for the cut gate design.

Figure 4.5.23.: Course of the detector gain and its components for the I_{PMOS} variation with fixed source potential V_{S}.

is used. A better approximation gives a second order polynomial formula

$$g_{\mathrm{q}}(I_{\mathrm{PMOS}}) = -0.003055 \cdot I_{\mathrm{PMOS}}^2 + 0.9592 \cdot I_{\mathrm{PMOS}} + 187.3$$

This is not surprising because the curve shape of g_{m} versus V_{G} for $V_{\mathrm{G}} < V_{\mathrm{Th}}$ in figure 3.3.14 equals a second order polynomial. Thus, it can be concluded that the short channel effects also influence the internal amplification of the DEPFET. It is for instance possible that

- the potential drop between source and drain leads to a non-equal distribution of the internal gate underneath the MOS gate. Its center of gravity is near the source. This may lead to an overestimation of the I_{PMOS} steering by the internal gate as the current density has its maximum at the drain due to the circular shape of the MOS gate.
- the fraction f of the electrons collected below the transistor channel Q_{iG}, which induce additional holes in the channel and thus modulate its conductivity, decreases for an increasing I_{PMOS}.

- for short channels the amount of Q_{iG}, which does also induce charge in source and drain, is underestimated anyhow.

As a result of the interplay of g_{m} and g_{q}, the detector gain g_{d} decreases with increasing I_{PMOS} because the change in g_{m} dominates the increase of g_{q}. Thus, for the detector operation a transistor current I_{PMOS} in the saturation region should be chosen to ensure stable performance. But a further increase of I_{PMOS} is not recommended as the internal amplification decreases and the thermal power induced in the detector increases.

4.6. Summary of the spectroscopic measurements

From the spectroscopic measurements of the DEPFET variants, insight in the following issues is gained:

- suitability of the different designs for Athena.
- size of the operation window with stable detector performance for several biasing voltages.
- accuracy of the prediction made by the electrical qualification measurements for the detector operation biasing.
- internal amplification of the DEPFET designs.
- readout speed limitations for the source follower configuration.

In general it can be concluded, that the cut gate, quasi linear and narrow gate designs are suited for Athena. The short gate design, that seemed promising after the electrical qualification was discovered to have a potential pocket and significant charge loss leading to a poor detector performance. Due to the inaccuracy of its spectroscopic measurement results discussed in section 4.5.3, the short gate device was excluded from all subsequent measurement series. The design first must be improved before effects of varied bias voltages or timing differences can be examined for it. It is suggested to round off the edges of the gate and clear gate. Hence, the influence of source and drain potential are similar at every point of the overlapping are and the potential pocket is expected to vanish.

All IS-devices were produced using a two step deep n-doping (DN0/2) for the formation of the internal gate. This production technology was revealed as weakness in section 4.5.2 because it lowers the potential barrier of the clear contact leading to charge loss. For further DEPFET productions the single step deep n-doping (DN1) is recommended to keep the energy resolution close to the physically given Fano-limit. Due to the charge loss, the lower readout noise ENC_{Meas} and higher detector gain g_{d} of the narrow gate design does not translate into a better energy resolution compared to cut gate and quasi linear structures.

For the chosen reference bias of section 4.3, the most borders of the operation windows presented in section 4.5.3 and the appendix A.2.1 are equal to the functionality limits. Just for the narrow gate structure the limit of the energy resolution

$FWHM_{\mathrm{Meas}} < 150$ eV is reached several times. Even though, the narrow gate design shows the largest operation windows for V_{ConS}, V_{GonS} and V_{DS}. Note, that for this design the fluctuation of the figures of merit is the highest. Thus, the narrow gate DEPFETs are most sensitive to any voltage variation. When the biasing voltages provided by Athena flight periphery are sufficiently stable, the narrow gate structure is recommended. Otherwise, the quasi linear design is recommended as it is the most stable and shows the largest operation windows for V_{CGoffS} and V_{CoffS}. In addition, it should be verified by simulations, how high the radiation damage of the WFI will be as the operation window of the narrow gate design will shift more rapidly than that of the quasi linear structure.

Independent of the DEPFET design, the backside voltage V_{B} should range between -110 V and -150 V and the ring voltage between -12 V and -17 V in order to deplete the device fully and form the potential funnel towards the internal gate as discussed in section A.2.1. Additionally, it was found, that an inner substrate bias V_{InS} of +0.3 V is sufficient to drain the surface leakage current from the polysilicon structures of the DEPFET.

The predictions made by the electrical qualification concerning the detector biasing are found to be useful. For an empty internal gate, the PMOS transistor of the DEPFET behaves for dynamic conditions of the spectroscopic measurements equal as for the quasi-static electrical measurements. This fact has been used for the investigation of the charge transconductance in section 4.5.4. For the biasing of the clear structure was obtained

$$\mathrm{mean}(V_{\mathrm{Conset}}) - 0.5\ \mathrm{V} \approx \max(V_{\mathrm{CoffS}})$$

$$\mathrm{mean}(V_{\mathrm{Conset}}) + 5\ \mathrm{V} \approx \min(V_{\mathrm{ConS}})$$

$$\mathrm{mean}(V_{\mathrm{CGonset}}) - 0.3\ \mathrm{V} \approx \max(V_{\mathrm{CGoffS}})$$

In order to ensure a complete clear process under dynamic conditions, a safety margin must be added to the predictions of the quasi-static electrical qualification.

During several measurement series it was found that the detector gain g_{d} as well as the charge transconductance g_{q} do not follow the theoretical expectations deduced from the transistor equations in section 2.2.3. The suggestion, that g_{d} is constant for varying V_{GS} is not supported by the measurement results of the V_{Gon} variation discussed in section A.2.1. The detector gain g_{d} is neither constant nor does it equal $\frac{1}{W \cdot L \cdot C'_{\mathrm{G}}}$ or $\frac{1}{A_{\mathrm{G}} \cdot C'_{\mathrm{G}}}$ for any used V_{GonS}. The detector gain also decreases slightly for an increasing transistor current I_{PMOS} despite the also increasing g_{q}. Additionally, the curve shape of g_{q} versus I_{PMOS} equals a second order polynomial instead of the expected square root formula as seen in section 4.5.4. This leads to several conclusions:

- g_{m} increases faster than g_{q} leading to a decrease of g_{d}.
- The effective transistor gate area cannot be determined using the design measurements.

- The DEPFET designs are no ideal long channel transistor but complex three-dimensional short channel devices.
- The potential drop between source and drain leads to a non-equal distribution of the internal gate underneath the MOS gate.
- The fraction f of the electrons collected below the transistor channel Q_{iG} decreases for an increasing I_{PMOS}.
- For short channels the amount of Q_{iG}, which does also induce charge in source and drain, is underestimated anyhow.

Thus, the dynamic behavior of the different DEPFET designs should be modeled with three dimensional simulations, in order to investigate the exact influence of the signal charge in the internal gate on the channel conductivity.

When for all varied timing parameter the operation minimum discussed in section 4.5.3 is used, a speed increase of 4% compared to the reference timing can be achieved. This is clearly not enough to increase the throughput of the detector sufficiently. Even with the parallelization of the readout and the signal multiplexing as well as increasing the general sequencing frequency the required $t_{\mathrm{Row}} = 2\ \mu\mathrm{s}$ for Athena [7] cannot be reached with the source follower readout. Instead the drain readout should be preferred because it does not need a settling time t_{Settle}.

5. Conclusion and outlook

With this study of the four different DEPFET variants not only designs suitable for Athena mission have been found but also a concise characterization procedure for DEPFET detectors has been defined. In addition, guidelines for expanded testing in order to increase the general knowledge of the DEPFET are given.

The required technology learning is provided e.g. with the discovery of the two step deep n-doping DN0/2 as weakness unless the p-doped barrier below the clear contact is reinforced with a higher implantation dose. Furthermore, limitations in the DEPFET design are revealed like the small feature size of the short gate design, which is likely to enhance short-circuits between the polysilicon layers. In order to provide high-quality wafer-scale detectors, this issues need to be solved whereas the production homogeneity over all devices and wafers is excellent and does not need improvement in the scope of Athena.

The predictions made by the electrical qualification concerning the detector biasing are found to be useful. For an empty internal gate, the PMOS transistor of the DEPFET behaves for dynamic conditions of the spectroscopic measurements equal as for the quasi-static electrical measurements. Only a small safety margin must be added to the predictions of the quasi-static electrical qualification for the use as operational parameters during spectroscopic measurements.

For Athena an ASIC for drain readout needs to be provided because even with the parallelization of the readout and the signal multiplexing as well as increasing the general sequencing frequency, the required $t_{\mathrm{Row}} = 2\ \mu\mathrm{s}$ cannot be reached with the source follower readout. As the DEPFET in drain readout configuration is more sensitive to biasing fluctuations, the spectroscopic characterization should be repeated for the cut gate, quasi linear and narrow gate design using the drain readout ASIC. For increased DEPFET behavior learning, several one-dimensional parameter sweeps are not enough, but on the contrary a time consuming multi-dimensional scan is mandatory. These measurements provide further insight in the behavior of the internal gate as the reference potential V_{S} of the PMOS is fixed for the drain readout.

At present, the complex three-dimensional structure of the DEPFET cannot be mapped with neither the ideal transistor equations nor existing models for short channel transistors. Nevertheless, the presence of short channel effects does not hamper the functionality of the DEPFET but make the clear assignment of measured effects to physical effects difficult if not impossible.

In the future more test structures should be provided for a study of the physical effects. Therefore, linear MOS transistors with several gate width to length combinations, circular MOS designs, linear DEPFET structures with and without adjacent

clear structure are needed. In order to investigate when short channel effects dominate the transistor behavior and how the clear structure influences the PMOS, these transistors should be characterized electrically. As result an analytical model of the circular MOS and the DEPFET will be gained. Additionally, a default reference structure like a cut gate device with $75\times75\mu m^2$ pixel size and fixed production technology should be defined and integrated on every wafer layout. The reference DEPFET can be used e.g. for the validation of new measurement setups or production technologies.

At present, this thesis, as the first systematic study of different DEPFET designs on die and detector level, shows the limitations of the current DEPFET assessment methods and provides improvement impulses for the starting device production for Athena.

A. Appendix

A.1. Electrical characterization

A.1.1. Contact list of short-circuit test

In order to screen for short circuits in a DEPFET matrix before the electrical characterization starts, the contacts are measured against each other as listed in table A.1.1.

Test number	+1 V	0 V
1	gate (G)	clear gate (CG)
2	gate (G)	clear (C)
3	gate (G)	drain (D)
4	gate (G)	ring (R1)
5	gate (G)	inner substrate (InS)
6	clear gate (CG)	clear (C)
7	clear gate (CG)	drain (D)
8	clear gate (CG)	ring (R1)
9	clear gate (CG)	inner substrate (InS)
10	clear (C)	drain (D)
11	clear (C)	ring (R1)
12	clear (C)	inner substrate (InS)
13	inner substrate (InS)	drain (D)
14	inner substrate (InS)	ring (R1)
15	drain (D)	ring (R1)
16	source (S) 1...64	gate (G)
17	source (S) 1...64	clear gate (CG)
18	clear (C)	source (S) 1...64

Table A.1.1.: Contact list short-circuit test: The applied potential polarity per test has to be respected in order to avoid opening parasitic pn-junctions or transistors.

A.1.2. Comparison of threshold determination methods for the saturation region

The second method for the threshold voltage extraction in the saturation region is the G1 function method, see figure A.1.1. The data of a pixel-wise measurement for a cut gate device is plotted as

$$G_1(I_{\mathrm{PMOS}}, V_{\mathrm{G}}) = V_{\mathrm{G}} - \frac{2}{I_{\mathrm{PMOS}}} \cdot \int_0^{V_{\mathrm{G}}} I_{\mathrm{PMOS}} dV_{\mathrm{G}}$$

This function is extrapolated using

$$G_1(I_{\mathrm{PMOS}}, V_{\mathrm{G}}) = V_{\mathrm{Th}} + \frac{1}{3}\sqrt{\left(\frac{2}{K_0}\right)} \cdot \sqrt{I_{\mathrm{PMOS}}}$$

with

$$K_0 \approx \beta$$

As [61, 62] do not mention where the extrapolation should start, the point of minimum slope is chosen.

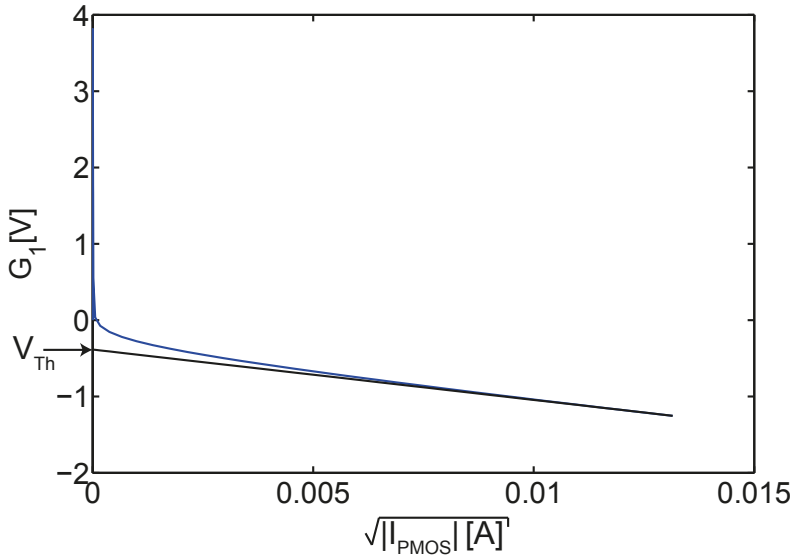


Figure A.1.1.: G1 function method for the pixel-wise measurement data of the cut gate (CuG) device that is also used for ESR in figure 3.3.5.

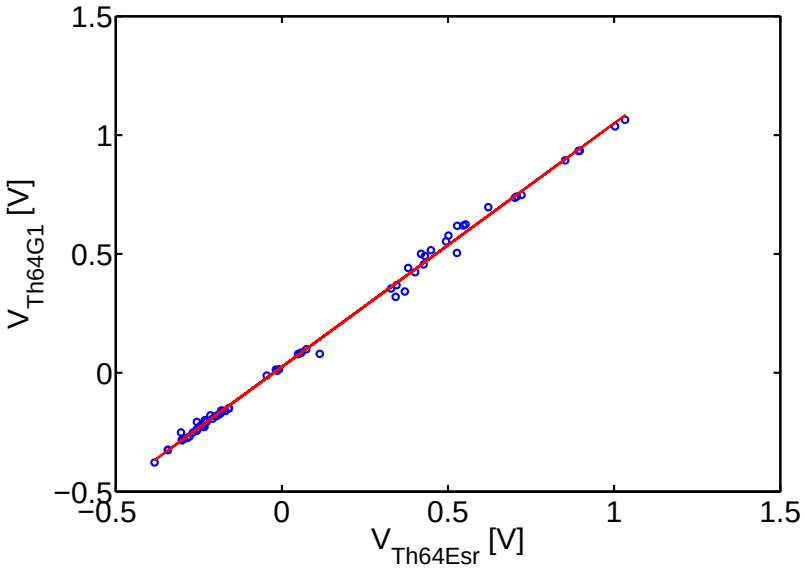


Figure A.1.2.: Blue circles represent the mean values of V_{Th64} for every device and both extraction methods. The red linear extrapolation with a slope of 1 shows that the G1 and the ESR extraction method nearly give the same results.

The comparison of the G1 function and ESR is shown in figure A.1.2 for V_{Th64} of the column-wise measurements from all 70 defect free devices. The linear extrapolation (red) going through (-0.025,0) and (0,0.025) in figure A.1.2 shows that the two threshold voltage extraction methods give nearly the same results. ESR seems more reliable because for the G1 function method it is not mentioned where exactly

the function should be linearly extrapolated. So ESR is the method of choice for extracting the threshold voltage of the DEPFET.

A.1.3. Transconductance

In contrast to the pixel-wise transconductance g_{m}, the transconductance of the column-wise measurements g_{m64} is determined at a column current of 300 µA, which is equal to an average pixel current $|I_{\mathrm{PMOS}}|$ of 4.7 µA. The determined g_{m64} values are presented in figure A.1.3 and table A.1.2.

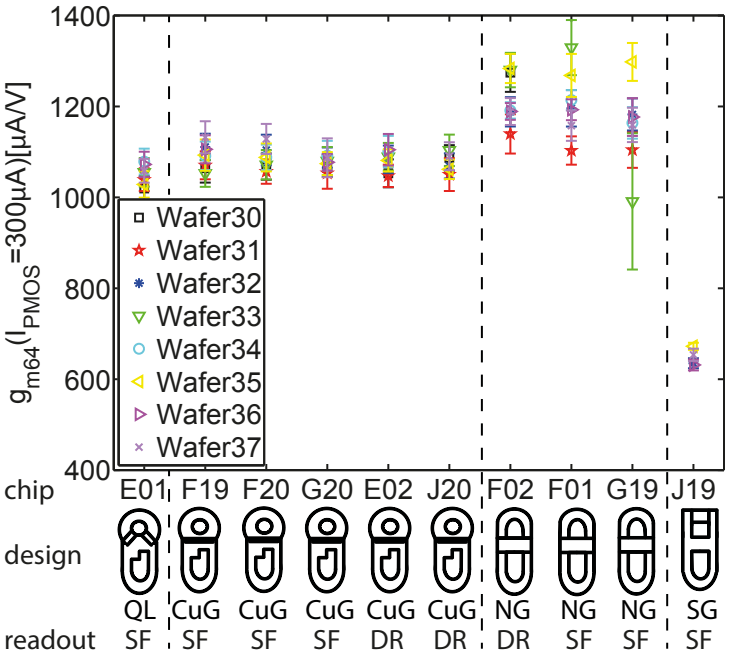


Figure A.1.3.: Mean column transconductance g_{m64} at $V_G(I = 300\ \mu A)$ for all 70 defect free IS devices. The standard deviation σ is indicated as error bar for every device.

As expected from the relation of gate width to length $\frac{W}{L}$ and as shown in section 3.3.2 for g_{m}, the devices range with design type. With about 648 $\frac{\mu A}{V}$ the short gate (J19) structures show the lowest g_{m64}, while with about 1181 $\frac{\mu A}{V}$ the narrow gate structures (F02, F01, G19) show the highest g_{m64}. Quasi linear (E01) and cut gate structures (F19, F20, G20, E02, J20) lie in between with about 1050 $\frac{\mu A}{V}$ and 1096 $\frac{\mu A}{V}$ respectively. Device G19 of wafer 33 shows a large deviation between the columns. This measurement has been repeated and confirmed, but so far no convincing explanation for the observed outlier has been identified.

Figure A.1.3 also shows that devices of wafers 30 and 31 have a slightly lower g_{m64} than dies from other wafers. The difference is caused by a 60 nm nitride layer above the gate oxide for wafers 30 and 31 instead of the usually used 30 nm nitride layer. A higher value of d_{Ni} leads to a smaller C'_{G}, which results in a lower g_{m64} for devices with thick nitride below the gate. Again for g_{m64} no quantitative comparison between

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}
g_{m64} $[\mu A/V]$	1096	58	1050	22	1181	85	648	19

Table A.1.2.: Average transconductance g_{m64} determined for the column-wise transfer characteristics summarized after table 3.3.2. Mean σ_{Die} is the average standard deviation of the parameter per die.

the theoretical prediction and the measured values is possible due to the presence of short channel effects.

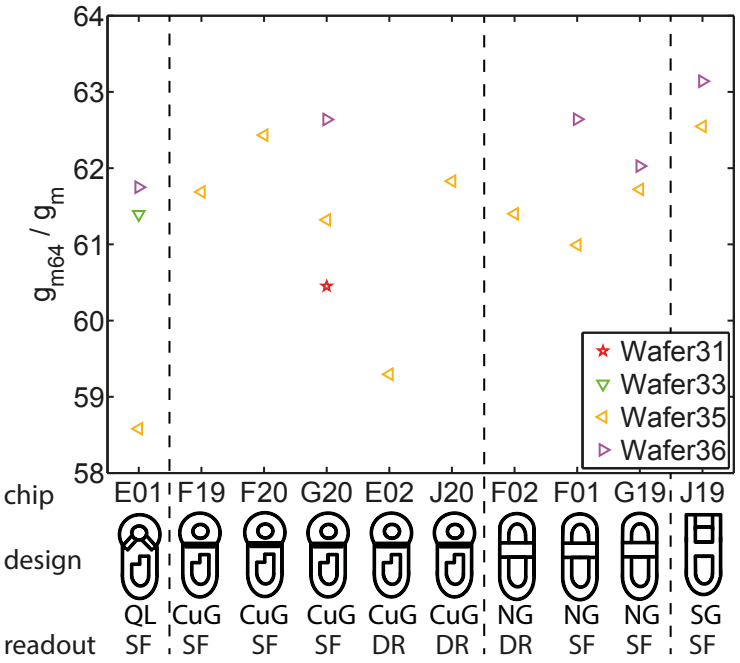


Figure A.1.4.: Average column-wise transconductance g_{m64} at $V_G(I = 300\ \mu A)$ divided by the recalculated average pixel-wise transconductance g_{m} at $V_G(I = 4.7\ \mu A)$.

In order to compare g_{m64} with g_{m}, the pixel-wise transconductance g_{m} has been recalculated for $V_G(|I| = 4.7\ \mu A)$. The quotient of the two averages is presented in figure A.1.4. Ideally the result would be 64 for all devices because one column contains 64 PMOS transistors. As the deviation for $|I_{\mathrm{PMOS}}| = 4.7$ µA is even worse than for 100 µA and only average values are used for the calculation, the quotient lies between 58 and 63. This shows, that column and pixel-wise measurements can be compared but the existing standard deviation must be kept in mind.

A.1.4. Theoretical curve fitting

For a cut gate (die F20), quasi linear (die E01) and narrow gate (die F01) structure of wafer 35 the same fitting routine was applied to the output characteristics as described for the short gate design (die J19) in section 3.3.3. The used and gained fitting parameter are presented in table A.1.3. The fitted curves for cut gate, quasi linear and narrow gate devices including the fitting errors are depicted in figures A.1.5

to A.1.7 in the same fashion as done for short gate in figure 3.3.25.

	Cut Gate	Quasi Linear	Narrow Gate	Short Gate
measured with V_{GS} * [V]	-2.91	-2.83	-1.92	-4.84
V_{Th} of I_{PMOS} (V_{GS}) [V]	-0.29	-0.16	+0.37	+0.17
resulting $V_{DS,sat}$ [V]	-2.62	-2.67	-2.29	-5.1
determined $1/\lambda$ [V]	+6.67	+6.13	+2.59	+3.27
$\beta_{theo}\,\frac{\mu A}{V^2}$	27.6 ± 0.80	23.6 ± 0.70	31.5 ± 1.00	9.1 ± 0.35
$\beta_{fit,lin}\,\frac{\mu A}{V^2}$	21.7 ± 0.15	21.0 ± 0.02	23.1 ± 0.25	7.5 ± 0.06
$\beta_{fit,sat}\,\frac{\mu A}{V^2}$	16.5 ± 0.05	15.3 ± 0.05	13.6 ± 0.04	3.3 ± 0.01
R^2_{lin}	0.9984	0.9985	0.9962	0.9940
R^2_{sat}	0.9891	0.9897	0.9970	0.9991

Table A.1.3.: Fixed fitting parameter and gained free parameter including its confidence interval for the output characteristics of all four designs. *V_{GS} is chosen such that at V_{DS} = -5 V a current $|I_{PMOS}|$ = 100 µA flows. As indicator for the goodness of the fits, the squared residual is given.

For all designs the β_{theo} calculated theoretically is greater than β of the fits and in addition $\beta_{fit,lin}$ is always greater than $\beta_{fit,sat}$. As expected, this indicates for all four design variants three-dimensional effects and short channel effects.

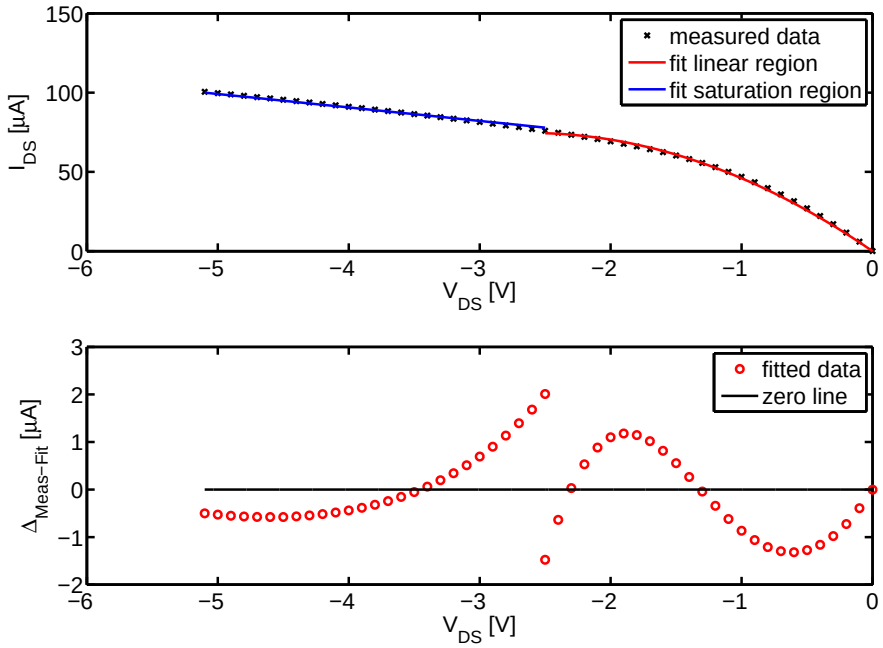


Figure A.1.5.: Output characteristics of cut gate (CuG) structure (die F20 of wafer 35) with fits in the linear region (red) and in saturation (blue). β is the free parameter and V_{GS}, V_{Th}, $V_{DS,sat}$ and $1/\lambda$ from table A.1.3 are used.

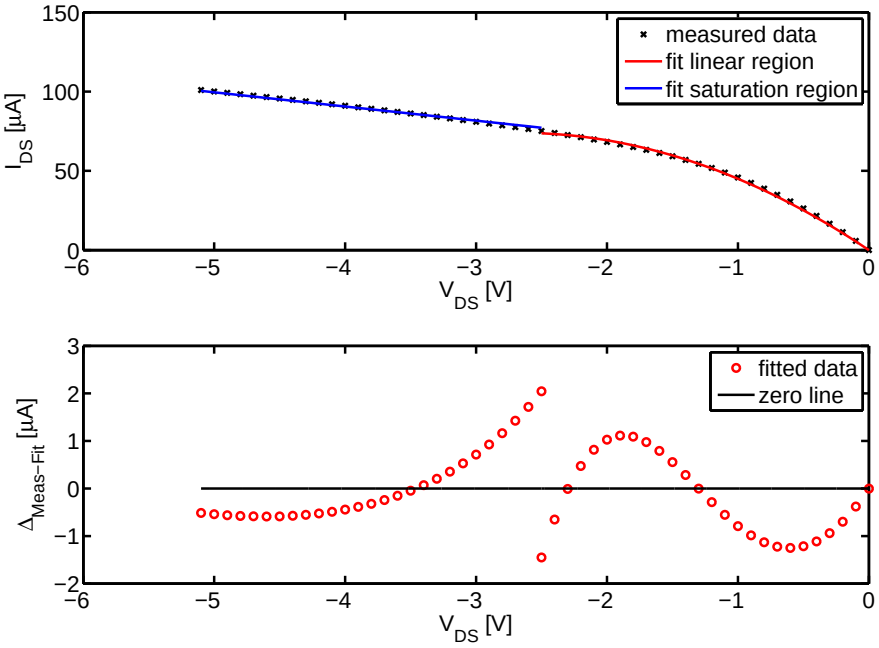


Figure A.1.6.: Fitting of the output characteristics of the quasi linear (QL) device E01 of wafer 35 in the linear region (red) and in saturation (blue).

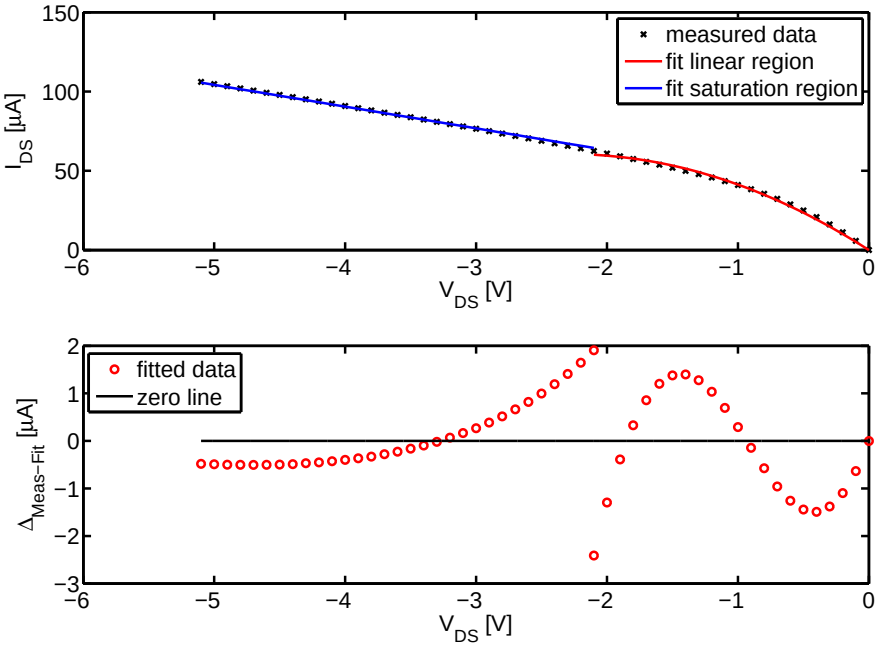


Figure A.1.7.: Fitting of the narrow gate (NG) output characteristics from die F01 of wafer 35 in the linear region (red) and in saturation (blue).

A.1.5. Clear characteristics

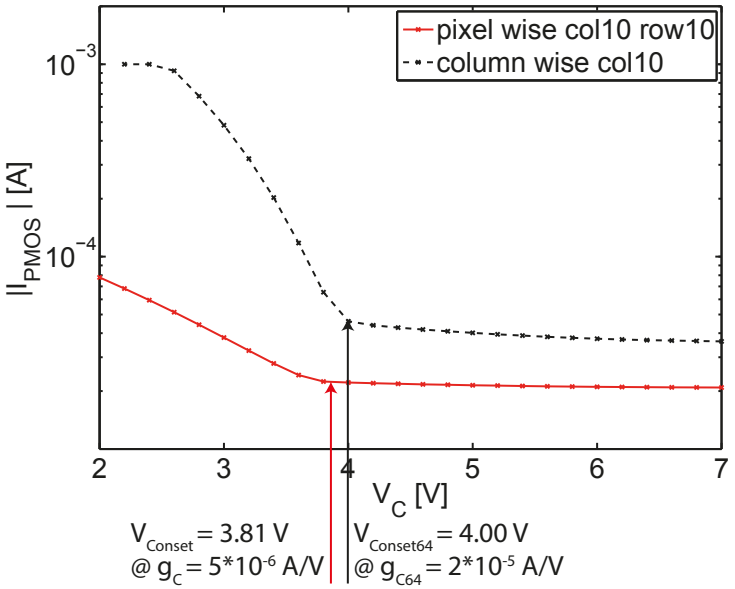


Figure A.1.8.: Comparison of pixel and column-wise measured clear characteristics for the cut gate (CuG) structure F20 of wafer 35.

In figure A.1.8 the pixel and column-wise measured clear characteristics for the cut gate structure F20 of wafer 35 are displayed as well as the extracted parameter V_{Conset} and V_{Conset64} respectively. In order to define the onset of the clear for the column-wise measurements, $V_{\mathrm{CGonset64}}$ for a ΔI_{PMOS} of 5% per measurement step of 0.2 V like for the single pixel characterization is determined. Therefore, the slope of the extraction point must be defined as $g_{C64} = -2 \cdot 10^{-5}\ \frac{\mathrm{A}}{\mathrm{V}}$. The results for V_{Conset64} for all 70 column-wise characterized dies are shown in figure A.1.9 and are summarized per design in table A.1.4.

The V_{Conset64} values group within a range of 1.3 V for all devices. Furthermore, devices of the same design type (see table 2.3.2), for instance F01 and G19 as narrow gate with source follower as well as F19, F20 and G20 as cut gate with source follower, have almost the same onset of the clear. It also seems, that the drain readout structures start to clear at lower V_{C} than the source follower devices (compare F01, G19 to F02 and F19, F20, G20 to E02, J20). However, this again is the result of the interchanged source and drain potential as described for V_{Th} in section 3.3.2.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}
$V_{Conset64}$ [V]	+4.08	0.02	+4.11	0.04	+3.29	0.04	+3.49	0.41

Table A.1.4.: Mean onset of the clear V_{Conset64} over all column-wise characterized dies from every DEPFET design according to table 3.3.2. Mean σ_{Die} is the average standard deviation of the parameter per die.

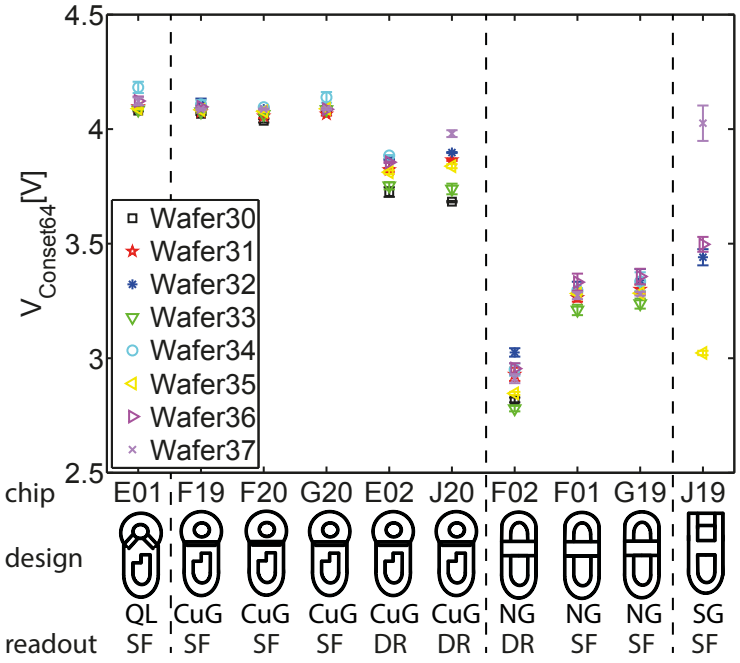


Figure A.1.9.: Average onset of the clear V_{Conset64}. The error bar marks the full width per die for the 70 column-wise characterized IS devices.

A.1.6. Clear gate characteristics

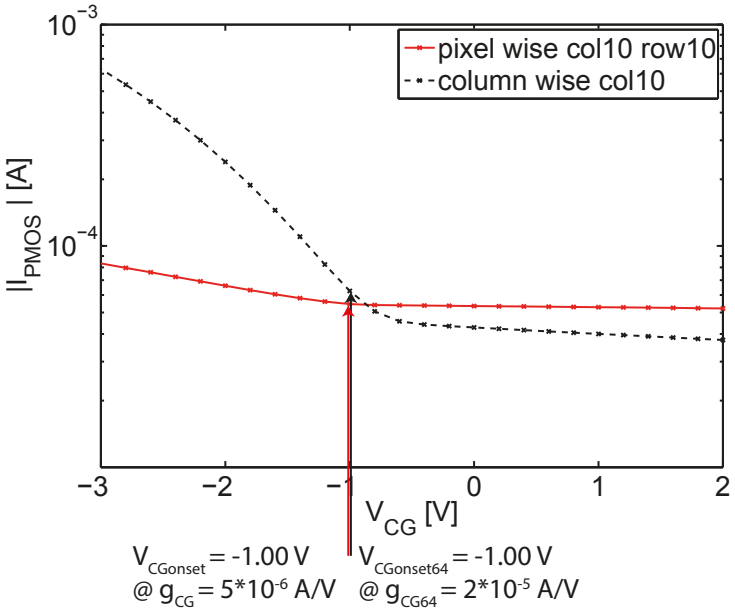


Figure A.1.10.: Comparison of pixel and column-wise measured clear gate characteristics for the cut gate (CuG) structure F20 of wafer 35.

As shown in figure A.1.10, the slope for the extraction of $V_{\mathrm{CGonset64}}$ needs to be adjusted to $g_{CG64} = -2 \cdot 10^{-5}$ $\frac{\mathrm{A}}{\mathrm{V}}$ like for V_{Conset64}. At this slope the current change

ΔI_{PMOS} per voltage step of 0.2 V is 5% as for the single pixel measurements.

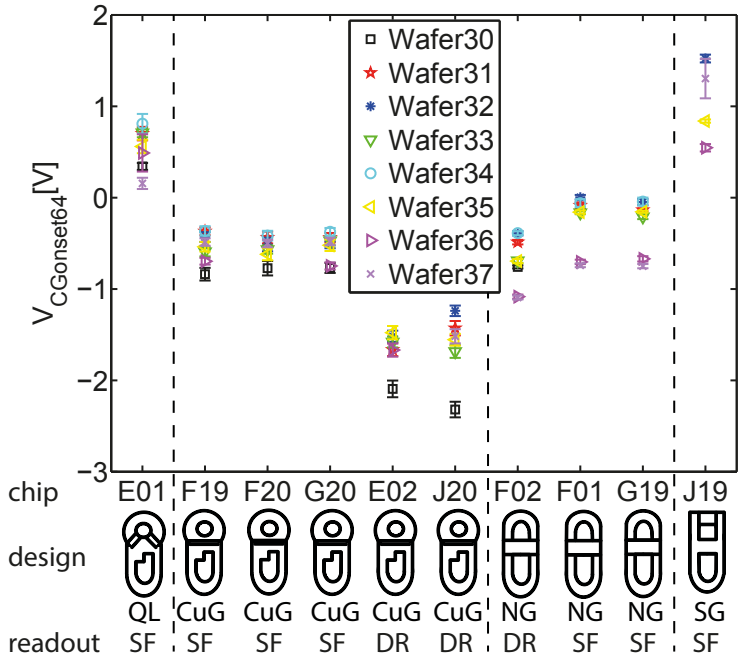


Figure A.1.11.: Average onset of the clear gate $V_{\mathrm{CGonset64}}$. The error bar marks the full width per die for the 70 column-wise characterized IS devices.

Figure A.1.11 shows that cut (F19, F20, G20) and narrow gate (F01, G19) structures have $V_{\mathrm{CGonset64}}$ of about -0.5 V and -0.3 V respectively except for their drain readout designs (E02, J20 and F02), which start to clear completely for much lower clear gate potentials. This issue was addressed before in section 3.3.2. $V_{\mathrm{CGonset64}}$ is summarized for all source follower structures according to table 3.3.2 in table A.1.5.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}	mean	mean σ_{Die}
$V_{CGonset64}$ $[V]$	-0.54	0.14	+0.54	0.23	-0.28	0.29	+1.05	0.44

Table A.1.5.: Mean onset of the clear gate $V_{\mathrm{CGonset64}}$ over all column-wise characterized dies from every DEPFET design according to table 3.3.2. Mean σ_{Die} is the average standard deviation of the parameter per die.

A.2. Spectroscopic characterization

A.2.1. Operation window

In addition to the V_{CGoff} measurement series presented in the main section 4.5.3, the results of the spectroscopic measurements for V_{Coff}, V_{Con}, V_{Gon}, V_{B}, V_{R1} and V_{InS} are given in the following sections. Note that in the graphs of the figures of merit only measurement points within the operation window are shown. The full range of measurements is given in the according tables.

Clear off voltage shift

The operation window shown in figure 4.5.15 not only displays the estimated boundaries for the V_{CGoff} variation but also for the V_{Coff} measurement series. The reference point for V_{CGoff} is with -3.19 V the same for all three DEPFET designs. For comparison the varied voltages are again referred to the source potential leading to a V_{CGoffS} between -2 V and -2.3 V depending on the design. This means the V_{Coff} scan has been done for the largest extent of the operation window with respect to the reference point depicted in table 4.3.1.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range V_{Coff} [V]	0.60↗2.40	-0.80↗2.40	-0.30↗1.80
injection starts @V_{Coff} [V]	0.60	-0.80	-0.30
significant increase of left side @V_{Coff} [V]	2.00	2.00	1.60
operation window V_{Coff} [V]	0.60↗2.40	-0.80↗2.40	-0.30↗1.60
operation window V_{CoffS} [V]	1.55↗3.35	0.23↗3.43	0.90↗2.80
mean V_{Conset} $[V]$	+3.81	+3.81	+3.11
ENC_{Meas} [e-]	5.43↗5.52	5.20↗5.28	4.83↗4.94
$FWHM_{\mathrm{Meas}}$ [eV]	136.1↗141.3	134.8↗147.3	134.6↗148.7
Offset [norm. Ref]	1.00	1.00↗1.02	1.00↗1.01
g_{d} [µV/e-]	3.82↗3.83	3.98↗4.01	8.07↗8.12
operation window ΔV_{Coff} [V]	1.8	3.2	1.9
$\Delta ENC_{\mathrm{Meas}}$ [e^-]	0.09	0.08	0.11
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	5.17	12.53	14.14
ΔOffset [norm. Ref]	0	0.02	0.01
Δg_{d} [µV/ e^-]	0.01	0.03	0.01

Table A.2.1.: Summarized results of the V_{Coff} variation. Δ equals the difference between highest and lowest measured value within the operation window.

The figures of merit for the V_{Coff} variation are shown in figure A.2.1 and are summarized in table A.2.1. The operation windows are terminated in the negative direction of V_{CoffS} by DEPFET functionality because of starting electron injection from the

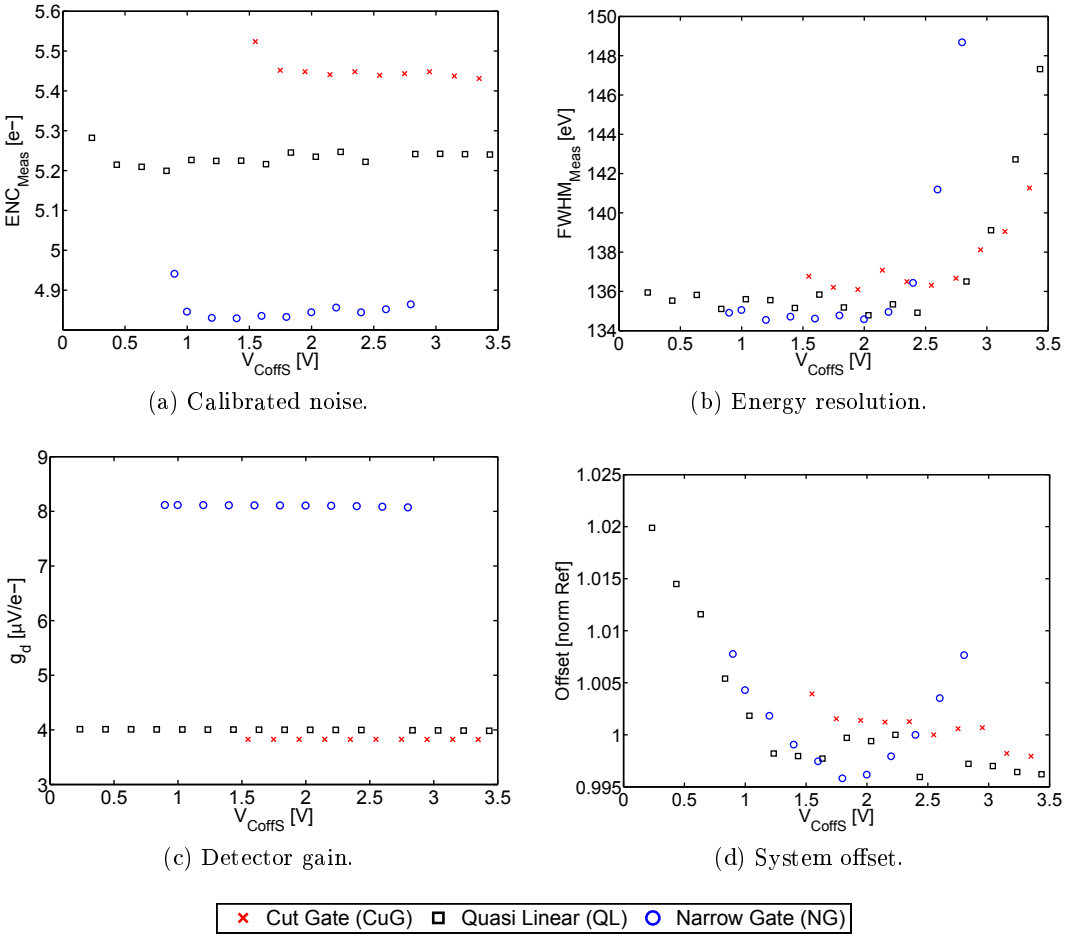


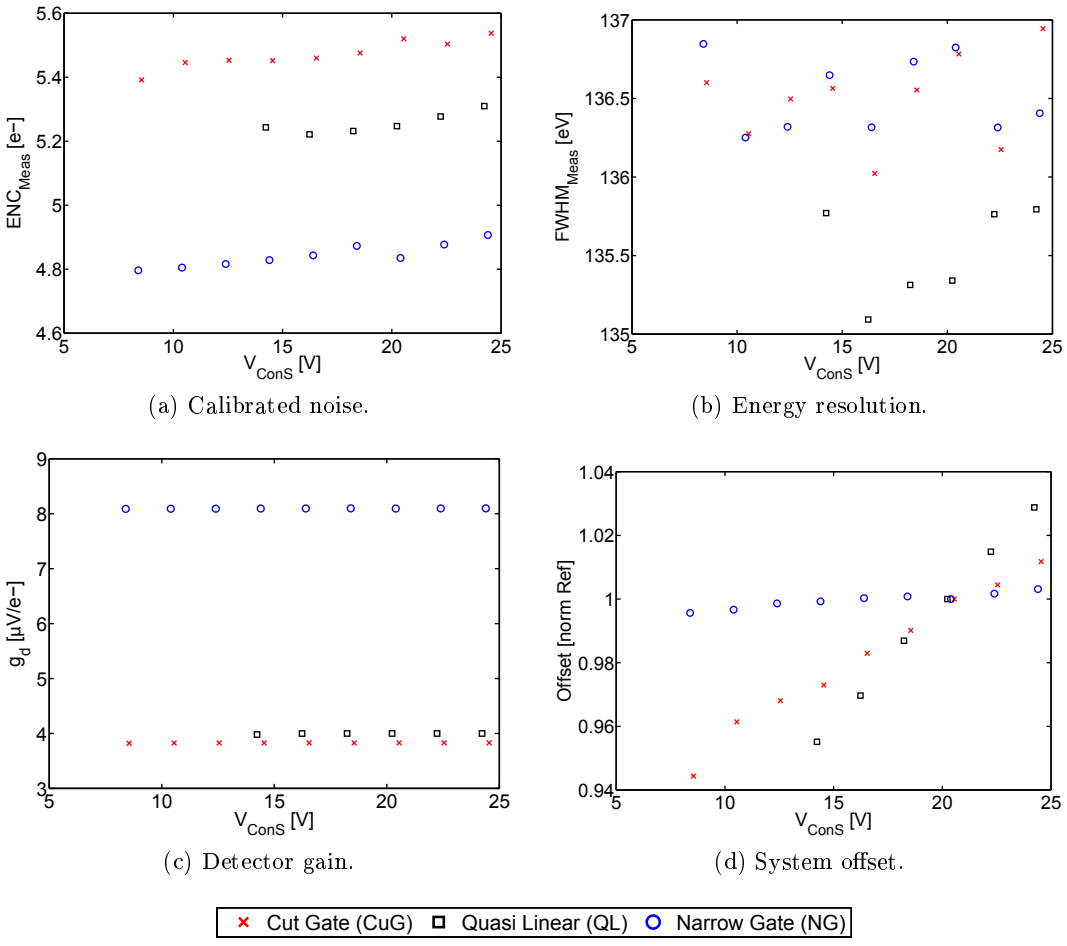
Figure A.2.1.: The figures of merit versus the clear off voltage referred to the source potential V_{CoffS}.

clear contact into the internal gate. This is indicated by the increase of the equivalent noise charge (see figure A.2.1a). In positive direction of V_{Coff}, the limit is given by the energy resolution $FWHM_{\mathrm{Meas}}$ (see figure A.2.1b) increasing above 150 eV. For too positive V_{Coff}, signal charge is drained into the clear contact during the charge accumulation phase owing to approaching the quasi-static determined onset of the complete clear V_{Conset}, which was discussed in section 3.3.4.

Like for the V_{CGoff} measurement series, the quasi linear design has with Δ V_{Coff} =3.2 V the largest operation span compared to 2.1 V for the narrow gate and 1.8 V for the cut gate design respectively. For the V_{Coff} measurement series as well as for V_{CGoff} and all others presented in the following sections, the measured noise ENC_{Meas} correlates to the detector gain g_{d} as explained in section 4.5.3. The variation of V_{Coff} seems not to effect the detector gain g_{d} because in figure A.2.1c g_{d} is constant for all three designs.

Clear on voltage shift

In contrast to the clear off voltage V_{CoffS}, the clear on voltage V_{ConS} must be more positive than V_{Conset}, which was presented in section 3.3.4, in order to drain all electrons from the internal gate during the readout sequence (see figures 2.2.17 and 4.3.1). In addition to the clear performance itself, V_{Con} plays an important role for the depletion of the DEPFET. The clear contact acts as the n+ contact necessary for the sidewards depletion described in section 2.2.3. That means, the detector volume is depleted completely during the clear process by V_{B} and V_{Con}. When the clear is switched to its off-state at V_{Coff}, the conditions for sidewards depletion are not fulfilled anymore and the detector volume slowly accumulates leakage charge. This charge is remove during the following clear cycle and the complete depletion is re-established. Due to the low leakage current of the DEPFET devices, a dynamic depletion is possible with the used operation timing. Owing to the dynamic operation, V_{ConS} is expected to differ clearly from V_{Conset}.



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

(d) System offset.

Figure A.2.2.: Results of the clear on voltage V_{ConS} variation for the three DEPFET designs. The system offset is normalized to the offset of the measurement with the reference bias.

The figures of merit for the clear on voltage V_{ConS} variation are shown in figure A.2.2 and summarized in table A.2.2. The lower limit for V_{ConS} is given by the non-complete charge removal from the internal gate. For all designs the most negative V_{ConS} for the dynamic detector operation is clearly more positive than the quasi-static determined onset of the complete clear V_{Conset}, see table A.2.2. As the upper limit $V_{\mathrm{Con}} = 24$ V is chosen in order to not push the limits of the SWITCHER ASICs. It can be seen that the quasi linear design has with $\Delta V_{\mathrm{Con}} = 10$ V the narrowest operation span of the three designs. This indicates, that the capacitive coupling between the clear gate and the PMOS gate, which does not exist for the quasi linear design, supports the development of an electrical connection between internal gate and clear contact during the clear phase of the readout.

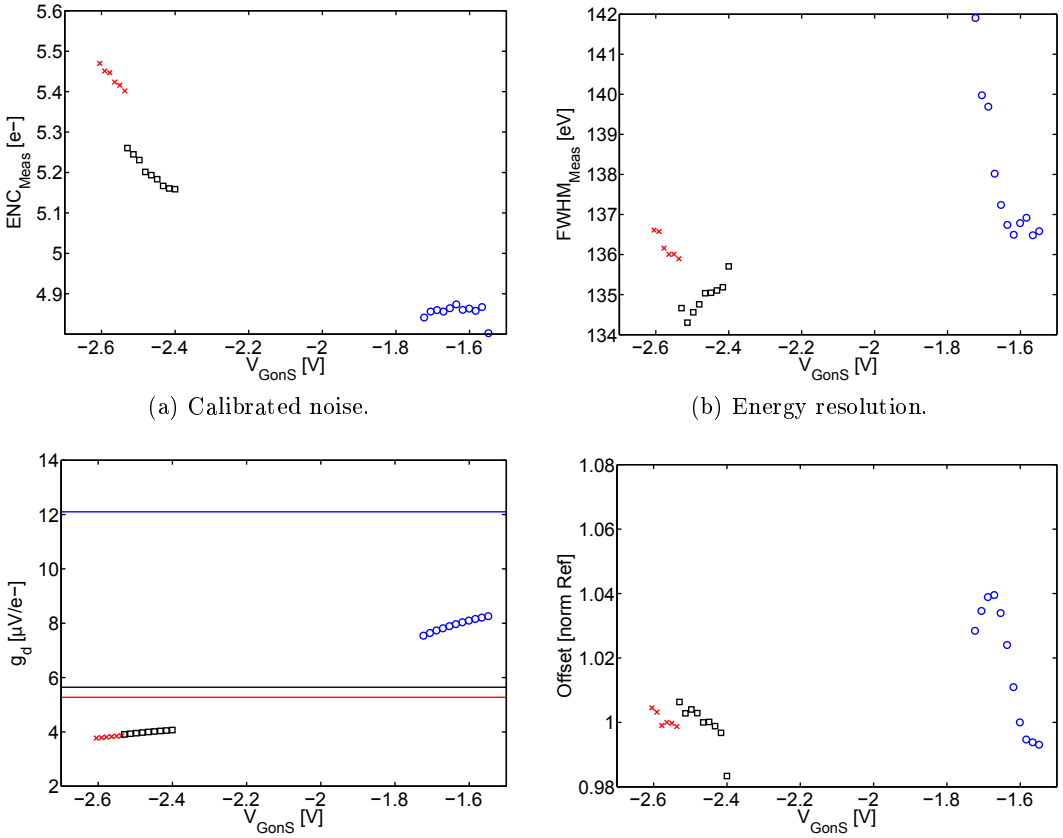
The equivalent noise charge increases slightly towards more positive V_{ConS} but it seems not to worsen the energy resolution. Hence, the $FWHM_{\mathrm{Meas}}$ in figure A.2.2a shows no tendency in its variation for all designs. Same as for V_{Coff}, the detector gain g_{d} is constant over the whole operation range of V_{ConS}. However, the offset increases for all designs with increasing V_{ConS} but with different slopes. The narrow gate design shows the smallest slope and the quasi linear the largest, as can be seen in figure A.2.2d. For higher V_{ConS} voltages the detector temperature increases about 1.5 °C due to electrical heating at resistivities. Thus, it is supposed that the leakage current increases slightly followed by the ENC_{Meas} and the offset. The slope of the increase correlates with the total amount of leakage current discussed in section 4.5.1.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range V_{Con} [V]	7.60↗23.60	7.20↗23.20	7.20↗23.20
operation window V_{Con} [V]	7.60↗23.60	13.20↗23.20	7.20↗23.20
operation window V_{ConS} [V]	8.55↗24.55	14.23↗24.23	8.40↗24.40
mean V_{Conset} $[V]$	+3.81	+3.81	+3.11
ENC_{Meas} [e^-]	5.39↗5.54	5.22↗5.31	4.80↗4.91
$FWHM_{\mathrm{Meas}}$ [eV]	136.0↗136.9	135.1↗135.8	136.3↗136.9
Offset [norm ref]	0.94↗1.01	0.96↗1.03	1.00
g_{d} [µV/ e^-]	3.82↗3.83	3.98↗4.00	8.09↗8.10
operation window ΔV_{Con} [V]	16	10	16
$\Delta ENC_{\mathrm{Meas}}$ [e^-]	0.15	0.09	0.11
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	0.9	0.7	0.6
ΔOffset [norm. Ref]	0.07	0.07	0
Δg_{d} [µV/ e^-]	0.01	0.02	0.01

Table A.2.2.: Summarized results of the V_{Con} variation. Δ equals the difference between highest and lowest measured value within the operation window.

Gate on voltage shift

In contrast to the clear gate and clear biasing, the gate on voltage V_{Gon} has a direct impact on the conductivity of the PMOS transistor channel. Hence, in case of the used source follower readout the source potential V_{S} does shift more than 0.8 V per 1 V V_{Gon} variation. As here again the varied voltage is referred to the source, a small operation range of V_{GonS} compared to the V_{Gon} range is the result. The figures of merit within the V_{GonS} operation window are depicted in figure A.2.3. The limits and parameter courses of the V_{Gon} variation are summarized in table A.2.3.



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain. The straight lines represent $\frac{1}{W \cdot L \cdot C'_{\mathrm{G}}}$ that should be equal to g_{d} after equation 2.2.34 for a linear transistor design.

(d) System offset.

Figure A.2.3.: Comparison of the figures of merit for the V_{Gon} variation. As done for all other applied voltages, V_{Gon} is referred to the source potential and written as V_{GonS} in order to allow the comparison of the DEPFET designs.

The limit of the V_{Gon} measurement series in negative direction is the input range of the ASTEROID ASIC for V_{S}. With increase of the channel conductivity a more negative V_{Gon} forces also a more negative V_{S} because the current through the DEPFET stays constant at 100 µA (see figure 4.3.3). As seen for the operation window of

V_{CGoff} and V_{Coff} in figure 4.5.13, the more positive V_{Gon} the smaller becomes the operation window for those parameters. The biasing of the clear structure is fixed to the reference potential of table 4.3.1. Thus, for a too positive V_{Gon} the reference V_{CGoff} and V_{Coff} are outside the possible operation window. This is the upper limit for V_{Gon}. The narrow gate design allows with $\Delta V_{\mathrm{Gon}} = 1$ V the broadest variation for the chosen reference bias.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range V_{Gon} [V]	-3.80↗-3.30	-3.90↗-3.10	-3.50↗-2.50
operation window V_{Gon} [V]	-3.80↗-3.30	-3.90↗-3.10	-3.50↗-2.50
operation window V_{GonS} [V]	-2.60↗-2.54	-2.53↗-2.40	-1.72↗-1.55
ENC_{Meas} [e^-]	5.40↗5.47	5.16↗5.26	4.80↗4.87
$FWHM_{\mathrm{Meas}}$ [eV]	135.9↗136.6	134.3↗135.7	136.5↗141.9
Offset [norm. Ref]	1.00	0.98↗1.01	0.99↗1.04
g_{d} [µV/ e^-]	3.77↗3.86	3.91↗4.07	7.54↗8.26
$\frac{1}{W \cdot L \cdot C'_{\mathrm{G}}}$ [µV/ e^-]	5.17	5.64	12.10
$\frac{1}{A_{\mathrm{G}} \cdot C'_{\mathrm{G}}}$ [µV/ e^-]	5.01	5.52	13.40
operation window ΔV_{Gon} [V]	0.50	0.80	1.00
$\Delta ENC_{\mathrm{Meas}}$ [e^-]	0.07	0.10	0.07
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	0.7	1.4	5.4
ΔOffset [norm. Ref]	0.01	0.02	0.05
Δg_{d} [µV/ e^-]	0.09	0.16	0.72

Table A.2.3.: Summarized results of the V_{Gon} variation. Δ equals the difference between highest and lowest measured value within the operation window.

Besides the clear structure biasing, the gate on voltage V_{Gon} has an impact on the DEPFET effective input capacitance C_{Det} and thus on the calibrated detector noise. The input capacitance represents the number of electrons needed in the internal gate to cause a conductivity change in the transistor channel that equals a certain voltage step at the external transistor gate

$$C_{\mathrm{Det}} = \frac{Q_{\mathrm{iG}}}{\Delta V_{\mathrm{Gon}}}$$

The capacitance can be determined using

$$\Delta V_{\mathrm{Gon}} = \frac{\Delta V_{\mathrm{S}}}{m}$$

with m as the slope of the source potential during V_{Gon} variation taken from table 4.3.2. The shift of the source potential can be replace by

$$\Delta V_{\mathrm{S}} = Q_{\mathrm{iG}} \cdot \frac{g_{\mathrm{q}}}{g_{\mathrm{m}}}$$

This leads to

$$C_{\mathrm{Det}} \propto \frac{g_{\mathrm{m}}}{g_{\mathrm{q}}}$$

According to equation 2.2.35, the equivalent noise charge of the detector and filter system ENC_{Filter} is proportional to C_{Det} when the leakage current contribution is neglected giving

$$ENC_{\mathrm{Filter}} \propto g_{\mathrm{m}}$$

As seen on the transfer characteristics of the PMOS transistor in section 3.3.2, the transconductance g_{m} of the transistor increases for more negative V_{GS}. Hence, ENC_{Meas} must increase also for more negative V_{GonS} like shown in figure A.2.3a. Though, for an ideal linear transistor it was claimed in equation 2.2.34 that

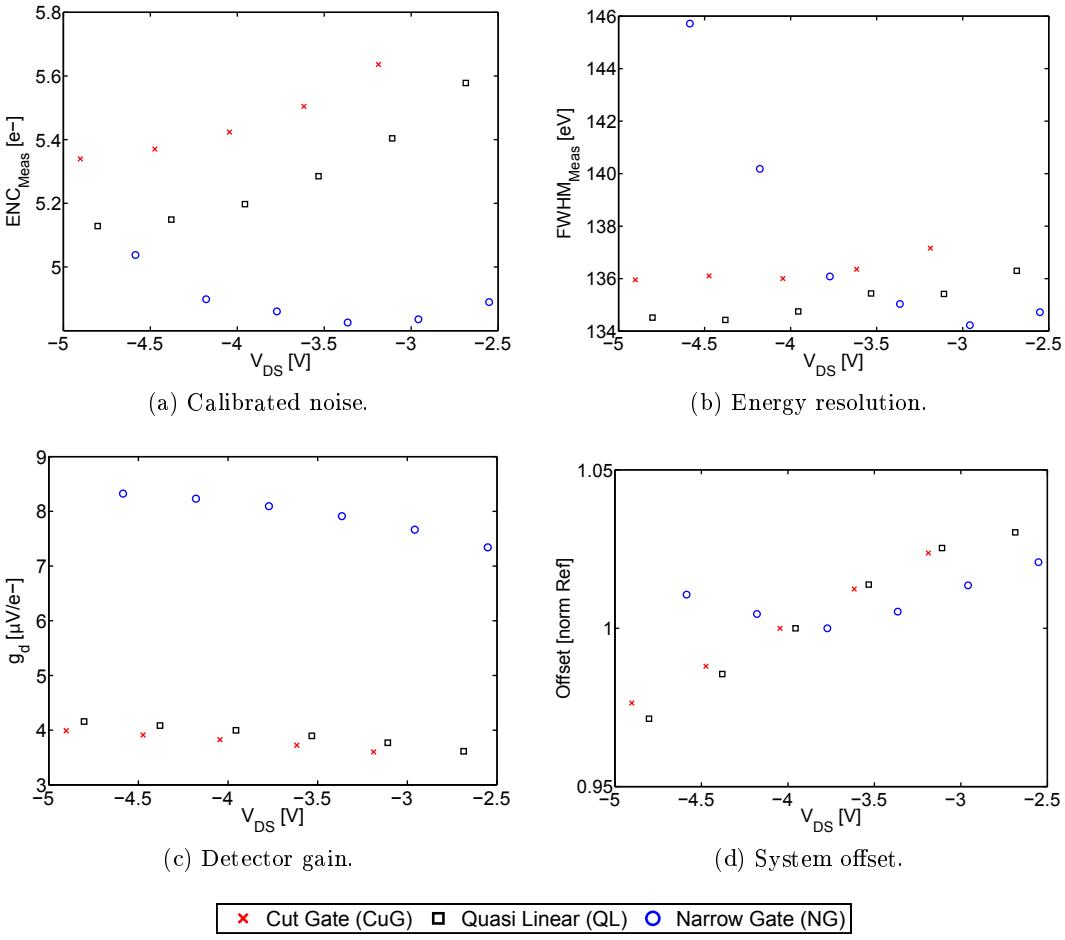
$$g_{\mathrm{d}} = \frac{g_{\mathrm{q}}}{g_{\mathrm{m}}} = \frac{f}{C_{\mathrm{G}}} = const.$$

This prediction cannot be confirmed when considering the measurement results in figure A.2.3c. The first striking feature in the figure as well as in table A.2.3 is that the detector gain g_{d} is not constant. Secondly, the gain g_{d} does not equal $\frac{1}{W \cdot L \cdot C'_{\mathrm{G}}}$ nor $\frac{1}{A_{\mathrm{G}} \cdot C'_{\mathrm{G}}}$ for any used V_{GonS}. This leads to several conclusions:

- g_{m} increases faster than g_{q} leading to a decrease of g_{d} for more negative V_{GonS}.
- The effective transistor gate area cannot be determined from the design dimensions as g_{d} does not equal the inverse gate capacitance neither calculated for a linear transistor nor for the real gate area of the different DEPFET designs.
- The DEPFET designs are no ideal long channel transistor but complex three-dimensional short channel devices.

Drain voltage shift

The second bias voltage besides V_{Gon} that has a direct influence on the PMOS transistor channel is the drain voltage V_{D}. The potential difference between source and drain V_{DS} control the hole velocity in the channel. Thus, a V_{D} variation in the source follower readout mode implicates also a variation of the source potential V_{S} for a fixed current $|I_{\mathrm{PMOS}}| = 100\ \mu\mathrm{A}$. But the source potential variation of about 0.16 V for a $\Delta V_{\mathrm{D}} = 1$ V is small compared to 0.8 V for V_{Gon}.



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

(d) System offset.

Figure A.2.4.: Comparison of the figures of merit for the V_{D} variation. V_{D} is referred to the source potential and written as V_{DS} in order to allow the comparison of the DEPFET designs.

The measurement range of V_{D} is limited in negative direction by the development of a high electric field in the channel region from all pixels that are switched off. It was found in [15], that electrons, which are generated thermally in this region, are accelerated by the field and free additional electrons due to collision similar to the avalanche effect. This charge leads to an increase of the leakage current and thus, worsens the measurement noise ENC_{Meas} and energy resolution $FWHM_{\mathrm{Meas}}$

because with equation 2.2.40 the noise contribution of the leakage current is

$$N_{\mathrm{Leak}} \propto \sqrt{I_{\mathrm{Leak}}}$$

For this reason the operation window ends with V_{D} = -6 V for all designs. For more positive V_{D}, the operation window is limited by leaving the saturation region of the PMOS transistor as $V_{\mathrm{DS}} > V_{\mathrm{DS,sat}} = V_{\mathrm{GS}}$ - V_{Th}. The figures of merit for the V_{D} variation are displayed in figure A.2.4 and summarized numerically in table A.2.4.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range V_{D} [V]	-6.00↗-3.00	-6.00↗-3.00	-6.00↗-2.50
operation window V_{D} [V]	-6.00↗-4.00	-6.00↗-3.50	-6.00↗-3.50
operation window V_{DS} [V]	-4.90↗-3.19	-4.80↗-2.69	-4.59↗-2.55
ENC_{Meas} [e^-]	5.34↗5.64	5.13↗5.58	4.83↗5.04
$FWHM_{\mathrm{Meas}}$ [eV]	136.0↗137.2	134.4↗136.3	134.2↗145.7
Offset [norm. Ref]	0.98↗1.02	0.97↗1.03	1.00↗1.02
g_{d} [µV/ e^-]	3.60↗3.99	3.62↗4.16	7.34↗8.32
operation window ΔV_{D} [V]	2.00	2.50	2.50
$\Delta ENC_{\mathrm{Meas}}$ [e^-]	0.30	0.45	0.21
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	1.2	1.9	11.5
ΔOffset [norm. Ref]	0.05	0.06	0.02
Δg_{d} [µV/ e^-]	0.39	0.54	0.98

Table A.2.4.: Summarized results of the V_{D} variation. Δ equals the difference between highest and lowest measured value within the operation window.

As seen for the quasi-static electrical qualification in section 3.3.2, the transconductance g_{m} increases from the linear to the saturation region. This means in the case of the dynamic V_{D} variation that g_{m} (V_{D} = -3.5 V) > g_{m} (V_{D} = -6 V) due to the also changing V_{GS}. For V_{Gon} has been shown in the previous section that equation 2.2.34

$$g_{\mathrm{d}} = \frac{g_{\mathrm{q}}}{g_{\mathrm{m}}}$$

has no constant gain value as a result. The relation between g_{m} and g_{q} is not static but dynamic and has more dependencies than stated in equations 2.2.31 and 2.2.33. Nevertheless, it is believed that

$$g_{\mathrm{d}} \propto \frac{1}{g_{\mathrm{m}}}$$

This validates a decreasing detector gain g_{d} for more positive V_{DS} shown in figure A.2.4c. Also deduced from the V_{Gon} variation is

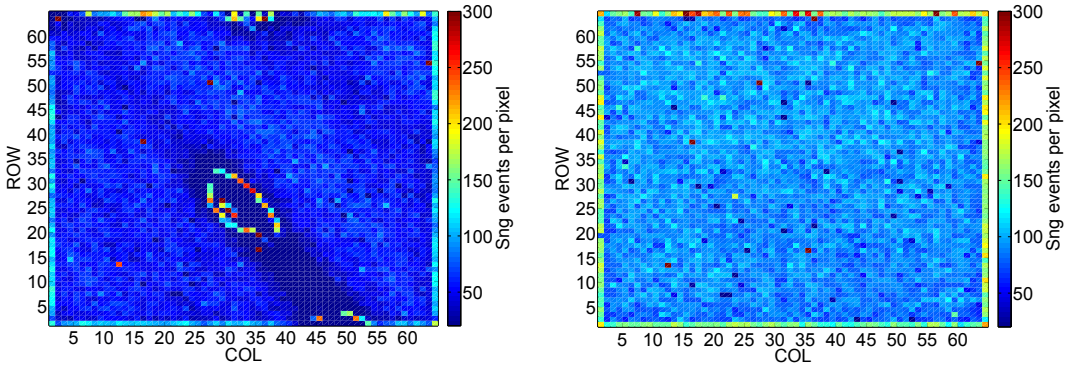
$$ENC_{\mathrm{Filter}} \propto g_{\mathrm{m}}$$

This indicates the increase of ENC_{Meas} for more positive V_{DS} as seen for the cut gate and quasi linear design in figure A.2.4a. On the other hand, the narrow gate

design shows a decrease of ENC_{Meas} for V_{DS} = -4.6 V up to -3.4 V and only for V_{DS} values more positive than V_{DS} = -3.3 V it shows the expected increase of ENC_{Meas}. It can be suspected that the starting voltage of V_{DS} for the increase of the leakage current due to impact ionization depends on the DEPFET gate design. Hence, the high field region develops in the narrow gate design for V_{DS} < -3.4 V so that the proportionality between ENC_{Filter} and g_{m} emerges for V_{DS} > -3.3 V. As expected, $FWHM_{\mathrm{Meas}}$ and the offset follow the ENC_{Meas}.

Backside voltage shift

The backside voltage V_{B} is essential for the sidewards depletion of the DEPFET as explained in section 2.2.3. Only when the backside voltage is sufficiently negative, the detector bulk is depleted completely and the potential funnel towards the internal gate is formed. Depending on the slope of the potential funnel, the signal charge cloud can spread over more pixels or is more focused on its way from the point of absorption to the internal gate. The backside voltage V_{B} must be chosen such, that in a measurement data set 100 to 150 single pixel hits are recorded for every pixel in order to have a valid gain determination (see section 4.4.2). The most positive V_{B}, for which the calibration is possible with reliable statistic, marks one limit of the V_{B} measurement series. In figure A.2.5 the single count maps for the lower limit of the backside voltage and the used reference biasing of the cut gate device are shown. It can be seen that for V_{B} = -100 V not all pixels reach the calibration limit and that the counts are not distributed evenly. Nevertheless, the gained spectrum for V_{B} = -100 V has a $FWHM_{\mathrm{Meas}}$ below 150 eV, this measurement point is considered to be within the operation window.



(a) Single count map for V_{B} = -100 V.

(b) Single count map for the reference bias V_{B} = -130 V.

Figure A.2.5.: Single count maps of the cut gate (CuG) design for different backside voltages V_{B}.

The other limit for the most negative V_{B} is defined by a peak broadening in the measured spectrum presented in figure A.2.6. It occurs because a too negative backside voltage pushes the charge cloud too close to the chip's surface leading to incomplete charge collection in the internal gate. Hence, the energy resolution decreases as the peak $FWHM_{\mathrm{Meas}}$ increases. The $FWHM_{\mathrm{Meas}}$ as well as the other figures of merit are shown in figure A.2.7. The comparison in numbers can be found in table A.2.5.

All designs show similar behavior for the figures of merit because the backside voltage is not related directly to the DEPFET design. The equivalent noise charge ENC_{Meas} increases for more negative V_{BS} due to the incomplete charge collection, which increases the standard deviation of the pixel calibration. Thus, the $FWHM_{\mathrm{Meas}}$ increases for more negative V_{BS}, too. If the measurement stability of section 4.4.3 is taken into account, for all designs the system offset as well as the detector gain g_{d}

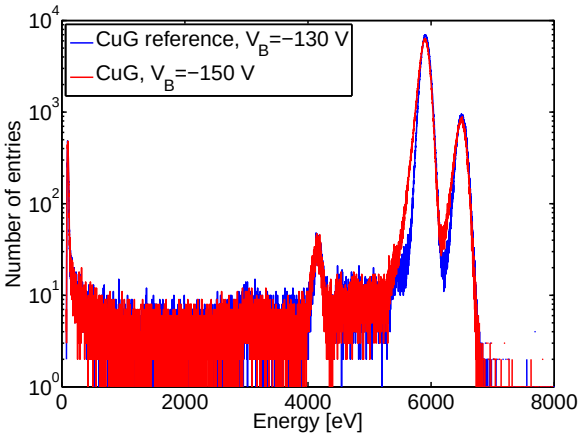


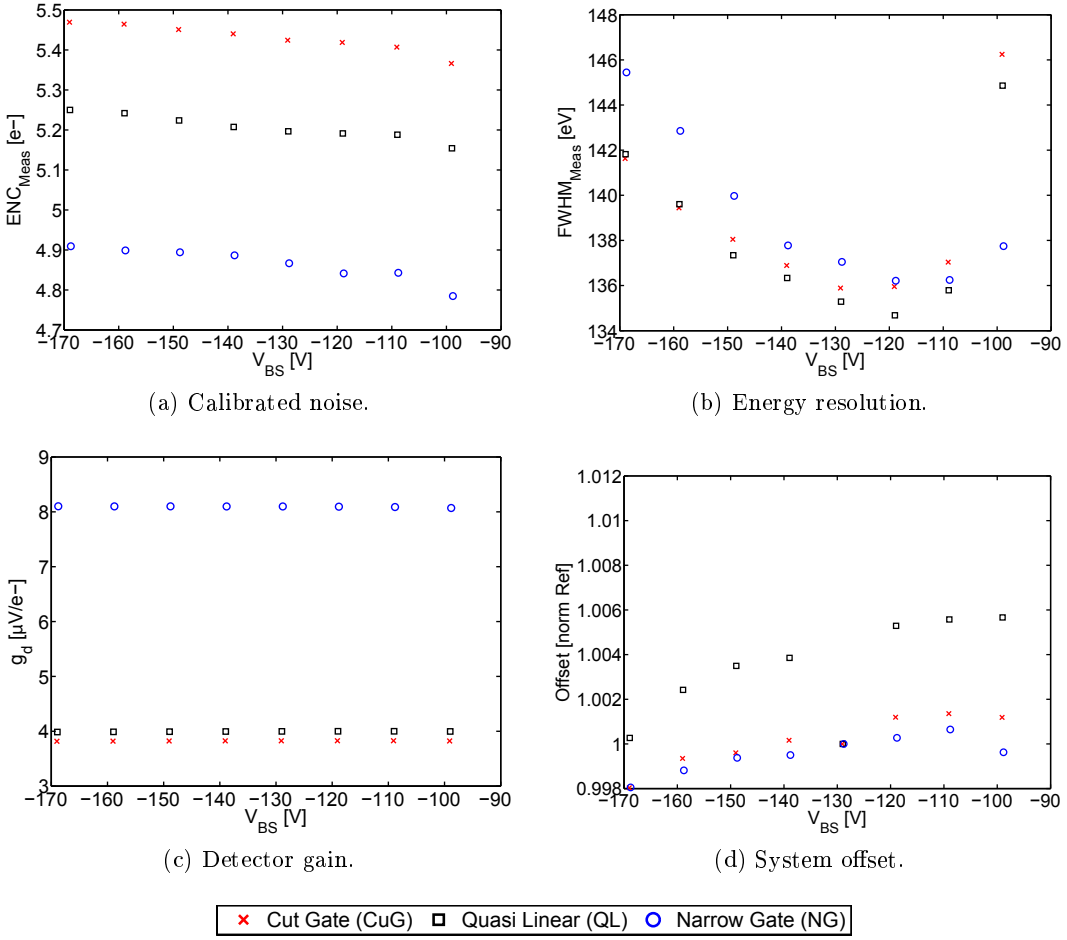
Figure A.2.6.: Impact of increasing backside voltage V_{B} on the all events spectrum for the cut gate (CuG) design.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range V_{B} [V]	-170.00↗-100.00	-170.00↗-100.00	-170.00↗-100.00
depleted completely @V_{B} [V]	-110.00	-110.00	-110.00
remarkable raise of left side @V_{B} [V]	-150.00	-150.00	-150.00
operation window V_{B} [V]	-170.00↗-100.00	-170.00↗-100.00	-170.00↗-100.00
operation window V_{BS} [V]	-169.01↗-99.09	-168.92↗-99.00	-168.76↗-98.82
ENC_{Meas} [e^-]	5.37↗5.47	5.15↗5.25	4.78↗4.91
$FWHM_{\mathrm{Meas}}$ [eV]	135.9↗146.3	134.7↗144.9	136.2↗145.5
Offset [norm. Ref]	1.00	1.00↗1.01	1.00
g_{d} [µV/ e^-]	3.82↗3.83	3.99↗4.00	8.07↗8.10
Single events [%]	31.2↘14.9	30.4↘14	31.6↘14.5
operation window ΔV_{B} [V]	70.00	70.00	70.00
$\Delta ENC_{\mathrm{Meas}}$ [e^-] [e^-]	0.10	0.10	0.12
$\Delta FWHM_{\mathrm{Meas}}$ [eV]	10.3	10.2	9.2
ΔOffset [norm. Ref]	0	0.01	0
Δg_{d} [µV/ e^-]	0.01	0.01	0.03

Table A.2.5.: Summarized results of the V_{B} variation. Δ equals the difference between highest and lowest measured value within the operation window.

does not change with a V_{BS} shift.

In table A.2.5 in addition to the common figures of merit, the percentage of single events is shown. As mentioned before, with a more negative V_{BS} the signal charge cloud is forced to the chips surface more quickly leading to less spread over several



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

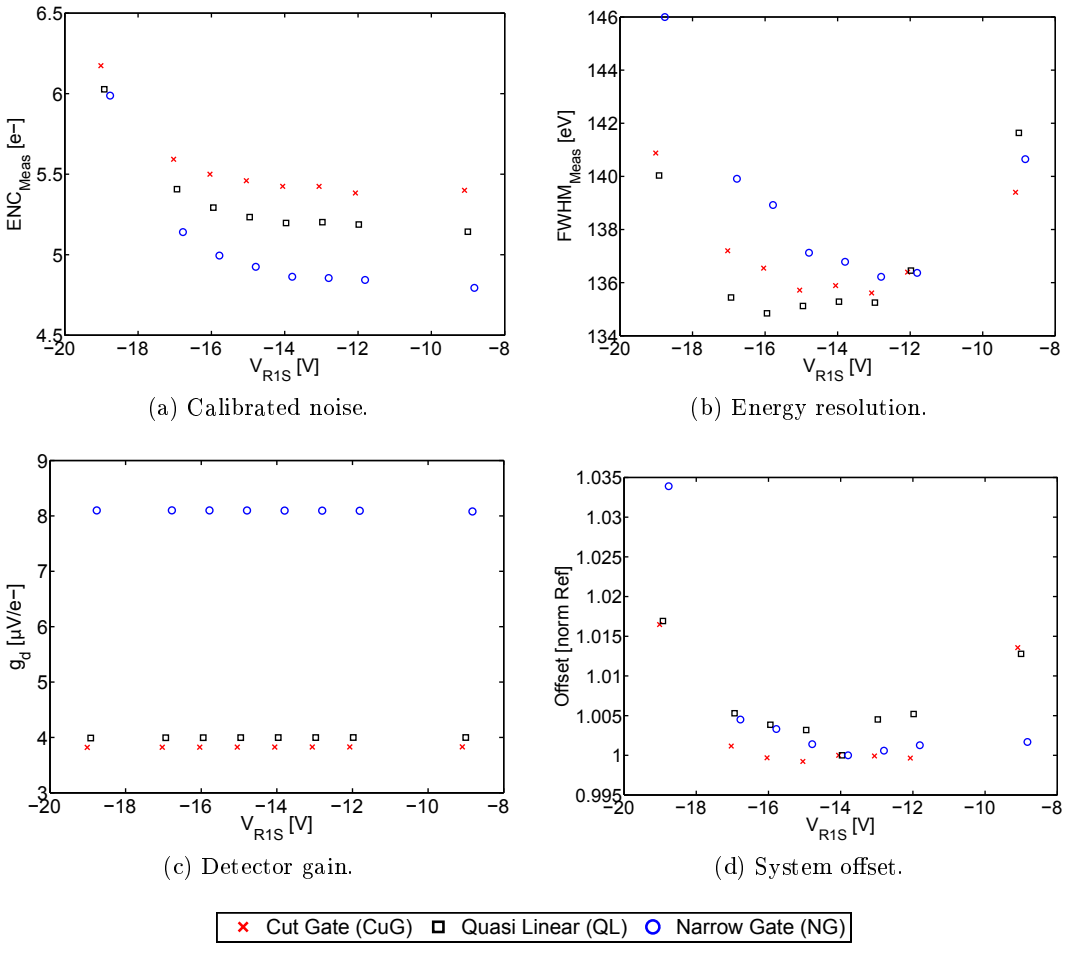
(d) System offset.

Figure A.2.7.: Results for the backside voltage measurement series. The backside voltage is referred to the source potential and marked as V_{SB}.

pixels. Thus, from the insufficiently depleted detector biased with V_{B} = -100 V to V_{B} = -170 V the number of single events per fixed measurement time doubles.

Ring voltage shift

The ring voltage V_{R1} is the counter part to the backside voltage V_B. The voltage V_B is the force for the charge cloud pointing from the back of the chip towards the front side. The ring separates the pixel potentials. Thus, the charge cloud is forced from the pixel borders towards the internal gate of the pixels. Like the backside voltage, the ring voltage must be sufficiently negative in order to establish the potential funnel. The more negative the backside voltage V_B is, the more positive V_{R1} can be. But when it is too positive, incomplete charge collection occurs due to a not fully established potential funnel. This limitation can be seen in the spectrum as an increase of the left side of the peak as shown for V_B in figure A.2.6. On the other hand a too negative V_{R1} separates the charge cloud at a greater distance from the chip surface leading to an increase of noise. In figure A.2.8 the figures of merit for the V_{R1} measurements are presented and in table A.2.6 the parameter are summarized numerically.



(a) Calibrated noise.

(b) Energy resolution.

(c) Detector gain.

(d) System offset.

Figure A.2.8.: Figures of merit for the ring voltage V_{R1} measurement series. The parameter are presented versus the ring voltage referred to the source potential V_{R1S}.

The limits of the ring voltage measurement series can be seen in the course of the

calibrated noise (figure A.2.8a) and energy resolution (figure A.2.8b). The operation window of V_{R1} is with 10 V equal for the three DEPFET designs but the figures of merits fluctuation is higher for the narrow gate device than for cut gate and quasi linear structure. The ring voltage has no direct impact on the internal gate or the PMOS leading to a constant detector gain g_d for all designs.

	Cut Gate	Quasi Linear	Narrow Gate
measurement range V_{R1} [V]	-20.00↗-5.00	-20.00↗-5.00	-20.00↗-5.00
remarkable raise of left side @V_{R1} [V]	-10.00	-10.00	-10.00
operation window V_{R1} [V]	-20.00↗-10.00	-20.00↗-10.00	-20.00↗-10.00
operation window V_{R1S} [V]	-19.01↗-9.09	-18.92↗-9.00	-18.76↗-8.83
ENC_{Meas} [e^-]	5.38↗6.17	5.14↗6.03	4.79↗5.99
$FWHM_{Meas}$ [eV]	135.6↗140.9	134.8↗141.6	136.2↗146
Offset [norm. Ref]	1.00↗1.02	1.00↗1.02	1.00↗1.03
g_d [µV/ e^-]	3.82↗3.83	3.99↗4.00	8.08↗8.10
operation window ΔV_{R1} [V]	10	10	10
ΔENC_{Meas} [e^-]	0.79	0.88	1.19
$\Delta FWHM_{Meas}$ [eV]	5.3	6.8	9.8
ΔOffset [norm. Ref]	0.02	0.02	0.03
Δg_d [µV/ e^-]	0.01	0.01	0.02

Table A.2.6.: Summarized results of the V_{R1} variation. Δ equals the difference between highest and lowest measured value within the operation window.

Inner substrate voltage shift

The inner substrate voltage V_{InS} is needed to drain surface leakage currents generated from the polysilicon ring, which is used as a potential separator. The V_{InS} voltage must be positive enough to attract electrons. Hence, the pixels do not drown in leakage current. For the three DEPFET designs V_{InS} is shifted from 0 V to +5 V as presented in table A.2.7. It was found that if the minimum necessary V_{InS} is applied a further increase of V_{InS} has no effect on any of the figures of merit. The minimum V_{InS} is 0.06 V more positive for the cut gate design than for the narrow gate and quasi linear structure. As the inner substrate is independent from the DEPFET designs no explanation can be given for the small difference.

	Cut Gate	Quasi Linear	Narrow Gate
V_{InS} [V]	0↗+5	0↗+5	0↗+5
minimum V_{InS} [V]	+0.26	+0.2	+0.2

Table A.2.7.: Result of the inner substrate voltage V_{InS} measurement series.

A.3. Paper

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Electrical characterization of different DEPFET designs on die level

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ABSTRACT: For the future X-ray astronomy project Advanced Telescope for High ENergy Astrophysics plus (ATHENA+) wafer-scale DEpleted P-channel Field Effect Transistor (DEPFET) detectors are proposed as Focal Plane Array (FPA) for the Wide Field Imager (WFI). Prototype structures with different pixel layouts, each consisting of 64 x 64 pixels, were fabricated to study four different DEPFET designs. We report on the results of the electrical characterization of the different DEPFET designs. The transistor properties of the DEPFET structures are investigated in order to determine whether the design intentions are reflected in the transistor characteristics. In addition yield and homogeneity of the prototypes can be studied on die, wafer and batch level for further improvement of the production technology with regard to wafer-scale devices. These electrical characterization measurements prove to be a reliable tool to pre-select the best detector dies for further integration into full detector systems.

KEYWORDS: Detector design and construction technologies and materials; X-ray detectors; X-ray detectors and telescopes

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1 Introduction

Since the DEpleted P-channel Field Effect Transistor (DEPFET) technology was proposed by Kemmer and Lutz in 1987 [1], it has developed into a detection module used in high energy particle physics [2] as well as space applications [3]. The DEPFET pixel matrices investigated here are prototypes for the Wide Field Imager (WFI) of the Advanced Telescope for High ENergy Astrophysics plus (ATHENA+) mission [4]. The WFI focal plane array will be a mosaic of a central chip with 256 x 256 pixels and four surrounding chips each consisting of 448 x 640 pixels covering in total an area of 120 mm x 120 mm. The ATHENA+ mission will explore super massive black holes and large scale structures of the universe. DEPFET detectors are well suited for this purpose as they provide an excellent detective quantum efficiency in the low energy X-ray band of 0.1 - 10 keV, and Fano limited spectral resolution can be reached. The DEPFET technology allows to easily scale the pixel size, hence it can be adapted to X-ray optics. The field of view is achieved by scaling the size of the pixel array. To improve the internal amplification of the detector as well as the readout speed, the layout of the DEPFET itself can be varied. In the following we will present results of the electrical characterization of four different DEPFET layouts. The obtained transistor properties reflect the design intention clearly and show a great homogeneity of the devices on die, wafer and batch level.

2 The DEPFET detector matrix

The investigated ATHENA+ prototype matrices consist of 64 x 64 square DEPFET pixels each. The size of one pixel is chosen to be 100 μm x 100 μm resulting in a die area of 10 mm x 12 mm including contact pads. The DEPFET in the center of every pixel, see figure 1, combines the charge storage and first amplification stage. The circular cutaway of the DEPFET is shown in figure 1. A DEPFET consists of two transistors. A P-channel Metal Oxide Semiconductor (PMOS) enhancement transistor is formed by the p+ doped drain and source contacts on n-bulk and the external Field Effect Transistor (FET) gate. A N-channel MOS (NMOS) transistor is formed by

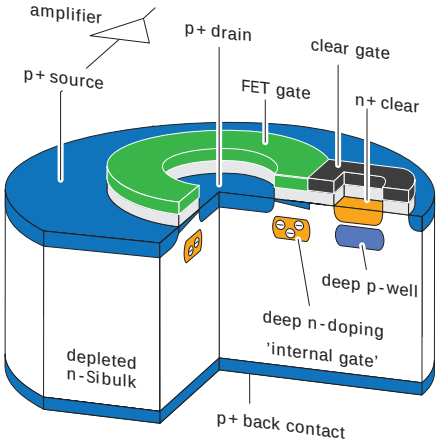

Figure 1. The circular DEPFET structure with sectional view of the internal gate (iG) and the clear (C) contact with deep p-well shielding towards the bulk [5].

the n doped region below the gate, the voltage controllable barrier called clear gate and the n+ doped clear contact, which is shielded towards the bulk by a p-implanted well. By looking at the DEPFET equivalent circuit depicted in figure 2 it becomes clear that a DEPFET matrix can be formed by arranging several single DEPFET pixels in a grid as done here for a 2 x 2 matrix. The clear, clear gate and gate contacts of all pixels are connected in rows and the source contacts in columns. The drain is biased globally as grid.

When appropriate bias voltages are applied to the front and back side of the DEPFET, the device is fully depleted. A potential minimum is created in the region of the internal gate below the external FET gate. If electron-hole pairs are generated in the depleted bulk, either by thermal generation or ionizing radiation, the holes will be driven to the back side. Electrons are collected in the internal gate. The potential minimum of the internal gate persists independent of the on or off state of the PMOS transistor. Hence, collected signal charge lingers in the internal gate regardless of the state of the transistor. When the PMOS transistor is switched on with a specific gate voltage, the transistor current is modulated by mirror charges induced by the collected signal electrons. In other words, the transistor is steered by the collected charge in the internal gate. This charge can be

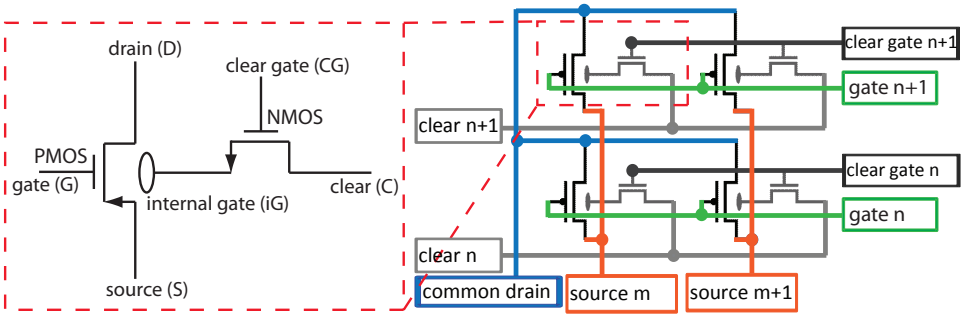

Figure 2. A DEPFET matrix can be formed by arranging several single DEPFET pixels in a grid and connecting their bias contacts in rows and columns.

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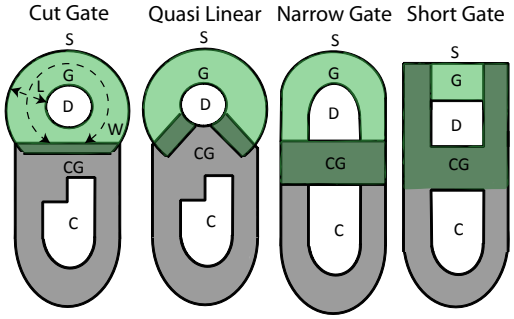

Figure 3. Schematic drawing of the four DEPFET design variants. The cut gate design is the well known baseline [6]. The gate area is highlighted green and the clear gate area gray. The darker green shade marks the overlapping region of those two areas.

Table 1. Relation between gate width W and length L for the different DEPFET designs.

	Cut Gate (CuG)	Quasi Linear (QL)	Narrow Gate (NG)	Short Gate (SG)
$\frac{W}{L}$	7.33	6.19	8.97	2.41

removed from the potential minimum by switching on the NMOS clear transistor. Using correlated double sampling the amount of stored electrons and thus the deposited energy can be measured.

Four DEPFET design variants, as shown in figure 3, have been studied. The DEPFET is embedded in the center of each pixel. In all variants the p+ drain is located in the center of the gate. The p+ source is the outer contact surrounding the gate. The differences of the variants are the size of n+ clear and p+ drain contacts, clear gate dimension and shape as well as overlapping area of gate and clear gate. A significant parameter to further describe the differences between the DEPFET designs is the relation of the gate width W to length L presented in table 1.

The cut gate design is used as well known default [6]. The quasi linear variant is the most similar to cut gate. The difference lies in a cut in the gate that allows the clear gate to touch the drain region without increasing the overlap between gate and clear gate. That results in a lower potential barrier between clear and internal gate. The lower barrier should accelerate the clear process and decrease the needed clear voltage. For narrow and short gate structures the gate area is minimized resulting in a higher amplification of the collected signal charge. A higher gain is expected to increase the signal to noise ratio of spectroscopic measurements.

3 Measurement setup for electrical characterization

Prototype devices from 10 different wafer positions of 8 wafers are electrically characterized using a setup adapted from earlier qualification measurements [6]. During the measurements the DEPFET matrix is contacted via a probe card and an automated probe head. The whole setup is located in a dark box in order to avoid light induced charge generation. The automated probe head and the probe card are connected to Toellner power supplies and Keithley source meter units. The connections of the setup parts can be changed using two Keithley programmable mainframes with 12 high speed relay multiplexer cards each providing 120 unipolar channels. Thus measurements

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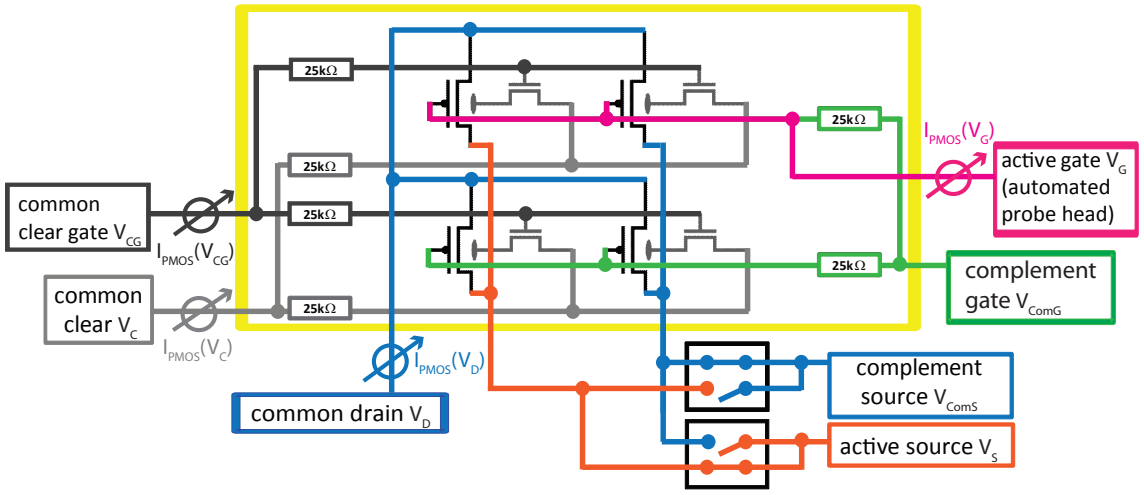

Figure 4. Connection schematic for the bench test with automated probe head for the example of a 2×2 matrix. Everything inside the yellow box is implemented on the DEPFET chip. The drain is biased as grid. Gate, clear and clear gate are biased row wise. One column of pixels is activated via the active source while the source potential of all other columns stays at drain potential applied through the complement source. Using the active gate a row of pixels is activated. The shown schematic is valid for all matrix sizes.

can be performed without shuffling plugs. In addition the setup can be easily adapted to other matrix sizes by using a matrix specific probe card.

The matrix is connected as shown in figure 4. In addition to the schematic shown in figure 2 the row wise clear, clear gate and gate contacts are connected on chip via bus structures to common contacts. Thus drain, clear, clear gate and gate are biased common for all pixels. One column of pixels is activated via the active source. All other columns stay turned off at so called complement source, which is equal to drain potential. Now one whole column can be measured. The automated probe head is used as active gate pulling the gate potential of just on row to on state. All other rows stay in off state defined by the complement gate because of the on chip resistors. Using active source and active gate allows to address a single pixel.

Before the detailed electrical characterization of the DEPFET matrices starts, a short-circuit test is performed. The short-circuit test screens for defective matrices. This is necessary because the DEPFET matrices are single defect sensitive. When a matrix passes this test, the transfer characteristic $I_{PMOS}(V_G)$, the output characteristic $I_{PMOS}(V_D)$ and the DEPFET specific clear $I_{PMOS}(V_C)$ and clear gate characteristic $I_{PMOS}(V_{CG})$ are measured column wise. This is used as quick check of the transistor properties for all defect free prototype matrices. The measurement time for one whole matrix is about 30 minutes. In addition several ATHENA+ matrices are tested pixel wise using the automated probe head as active gate, applying the biasing depicted in table 2. For pixel wise measurements the measurement time extends to number of rows multiplied by 30 minutes. This results in our case in 32 hours per die containing 64 x 64 DEPFETs. The timing of the measurements is chosen such that quasi static conditions are ensured. The measurement precision of the setup is 0.5 nA.

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Table 2. Biasing conditions for active gate V_G and complement gate V_{ComG}, drain V_D, active source V_S and complement source V_{ComS}, clear V_C and clear gate V_{CG} for the ATHENA+ prototype matrices using the automated probe head. The arrow emphasizes the direction of voltage variation. The reference for all voltages is the source potential. For $I_{PMOS}(V_D)$, $I_{PMOS}(V_{CG})$ and $I_{PMOS}(V_C)$ the active gate voltage is chosen such that a PMOS current of 100, 50 or 20 μA is forced through the DEPFET.

	$V_D = V_{ComS}$	V_S	V_{ComG}	V_{CG}	V_C	V_G
$I_{PMOS}(V_G)$	-5 V	0 V	+5 V	+5 V	+10 V	+1.5 V↘-4.5 V
$I_{PMOS}(V_D)$	0 V↘-5.1 V	0 V	+5 V	+5 V	+10 V	$V_G(I \approx 100\ \mu A)$
$I_{PMOS}(V_{CG})$	-5 V	0 V	+5 V	+2 V↘-3.6 V	+10 V	$V_G(I \approx 50\ \mu A)$
$I_{PMOS}(V_C)$	-5 V	0 V	+5 V	+5 V	+7 V↘+0 V	$V_G(I \approx 20\ \mu A)$

4 Results and discussion

A typical data set of the transfer characteristics for the 4 DEPFET variants is depicted in figure 5a. As expected the curve shapes are dependent on the relation of gate width W to length L of the design variants. For every device the transconductance g_m, the gate voltage for the defined on state $V_{on} = V_G(I = 100\ \mu A)$ and the threshold voltage V_{th} are extracted from the transfer characteristic. Comparing these parameters among the devices, as shown for V_{th} in figure 5b, proves similar behavior within every design group. The figure shows also that the performance parameter values obtained with the pixel wise and the column wise measurement method are very close to each other. Thus, for estimating operational parameters, it is sufficient to use the quicker measurement routine without automated probe head. Nevertheless, to investigate the homogeneity and study details of the layout variants, the pixel wise test is essential as shown in figure 7.

A gate voltage variation $\Delta V_G(I = 100\ nA)$ with less than 0.4 V within every device demonstrates an excellent homogeneity. The outstanding production homogeneity is also illustrated by a

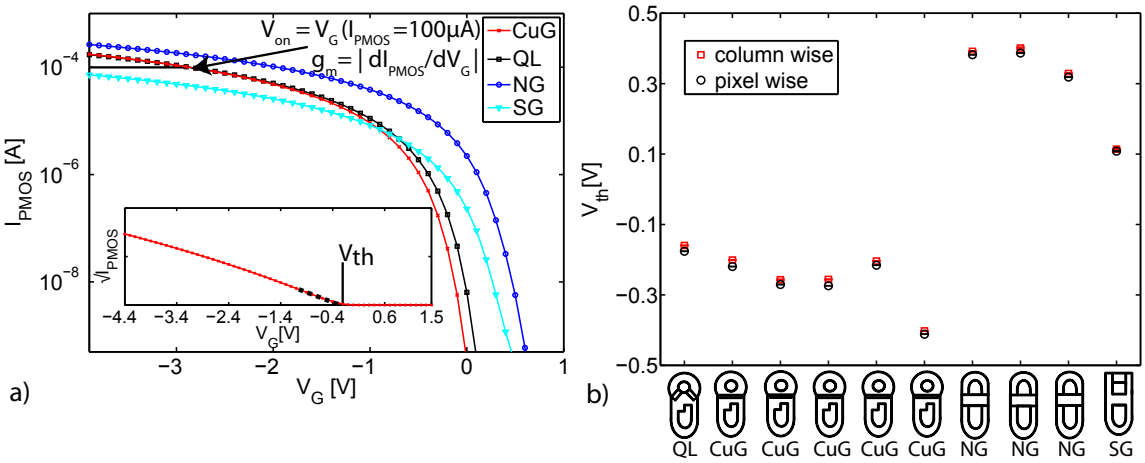

Figure 5. a) The transfer characteristic of one representative pixel for each design from the same wafer with the parameter extraction points. The inset shows the determination of the threshold voltage V_{th} using the extrapolation method for the cut gate (CuG) characteristic. b) Comparison of V_{th} deduced for all 10 devices of a single wafer using the column wise measurement as well as the pixel wise measurement with the automated probe head.

Table 3. Mean parameter values determined over all chips from every DEPFET design. Mean Δ_{Die} is the average full width of the parameter per die.

	Cut Gate		Quasi Linear		Narrow Gate		Short Gate	
	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}	mean	mean Δ_{Die}
V_{th} $[V]$	-0.31	0.16	-0.21	0.15	0.38	0.22	0.22	0.34
V_{on} $[V]$	-2.92	0.23	-2.93	0.23	-1.89	0.31	-4.88	0.58
g_m $[\mu A/V]$	65.8	4.73	63.2	3.55	74	5.9	29.4	2.71
$1/\lambda$ $[V]$	6.6	0.8	6.3	0.7	2.5	0.45	3.4	0.38
g_0 $[\mu A/V]$	8.2	1.54	8.3	1.5	13	3.3	11.3	2.13
V_{Con} $[V]$	3.81	0.12	3.81	0.13	3.11	0.2	2.75	0.16
V_{CGon} $[V]$	-0.92	0.72	0.02	0.68	-0.68	0.36	-0.19	0.55

gate length variation ΔL of less than 2.3 % for all designs despite of short gate with $\Delta L = 3.9$ %. The gate length variation ΔL is deduced from the variation of I_{PMOS} in the ohmic region among all pixels of one device for a fixed gate voltage. As expected for the small gate design, technology tolerances have a higher impact on the transistor behavior and cause higher variations of a performance parameter per die. It was already shown for Mercury Imaging X-ray Spectrometer (MIXS) macropixel matrices [3] that our readout and steering ASICs can cope with these tolerances. As no systematic difference between various wafers was observed, it is sufficient to compare parameter mean values for the complete batch for each layout. The values are shown in table 3 with the associated average full width per die.

For short gate devices a more negative gate voltage V_{on} must be applied to reach the on state of the transistor. But the less steep slope g_m of the curve compensates the higher production variation. That means, the applied gate voltage V_{on} should lead to less deviation in the transistor current from pixel to pixel than for the other designs. This ensures a homogenous amplification of the matrix. The amplification results from the relation of the current modulation from the collected charge g_q to the transconductance of the transistor channel g_m. Thus, lowering g_m can increase the DEPFET gain, and therefore the short gate structure is expected to have the highest amplification.

The performance parameters extracted from the output characteristic of the DEPFET PMOS are the conductance g_0 and the inverse channel length modulation factor $1/\lambda$, see figure 6a. The higher this factor, the smaller is the pinch-off of the channel in the saturation region with more negative V_D. The modulation of the channel length changes g_m, g_q, I_{PMOS} and the transistor capacitance. These variations influence the DEPFET gain and the timing as well as the readout noise. Detailed information about the influence of the pinch-off must be evaluated with dynamic detector measurements and can not be determined with static electrical tests.

As mentioned in section 2, the clear structure is needed to empty the internal gate during readout. For which clear and clear gate voltages the electrons collected in the internal gate are fully removed, is investigated by measuring the DEPFET specific clear and clear gate characteristic. A typical data set for $I_{PMOS}(V_C)$ is depicted in figure 6b. The clear gate is set open with +5 V. Thus, there is no potential barrier between internal gate and clear contact. When the clear voltage becomes too low, the PMOS current rises because of leakage current accumulating in the potential minimum. The onset of the complete clear V_{Con} is defined at a slope of $g_c = 5 \cdot 10^{-6}$ A/V representing a PMOS current change of 5 %. Likewise graphs are extracted from the clear gate

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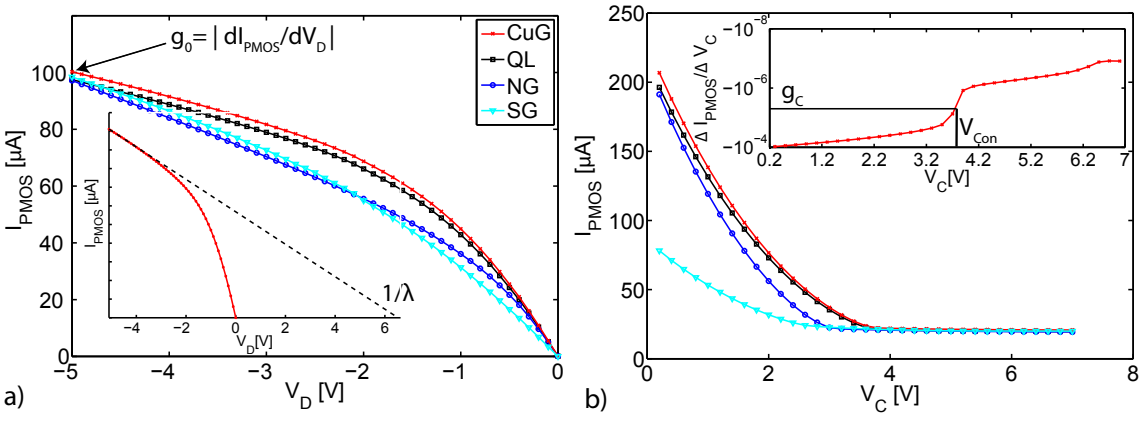

Figure 6. a) Representative output characteristic for all 4 designs. The pixel are chosen from the same wafer. The inset shows the determination of the inverse channel length modulation factor $1/\lambda$ for the characteristics of the cut gate (CuG) pixel. b) Representative clear characteristic for all 4 designs. The inset shows the determination of the clear onset voltage V_{Con} at $g_c = 5 \cdot 10^{-6}$ A/V for the cut gate (CuG) pixel.

characteristic. As intended for the quasi linear structure the potential barrier between clear and internal gate is much lower than for the cut gate device, as evidenced by a positive V_{CGon} in table 3. The short gate structure shows a more positive V_{CGon}, too.

In figure 7 the maps of the onset voltage of the clear V_{Con} for several devices with respect to their wafer position are shown. Because of the different DEPFET layouts, V_{Con} is normalized to the minimum value for every die. A concentric structure is visible for all devices with varying markedness for the different DEPFET designs. It is supposed that this structure is a result of the resistivity variation of the high ohmic (3500 - 7000 Ωcm) float zone silicon wafer material [3] with a diameter of 150 mm. It can be seen that by using the automated probe head fine structures and technology influenced effects like bright or dark pixel can be revealed, which cannot be seen with the much faster column wise measurements. Hence, depending on the required degree of detail and the available measurement time, the appropriate measurement set can be chosen.

5 Summary and outlook

The measurements show a great homogeneity within every device, wafer and batch. For all extracted performance parameters the devices cluster with design. That demonstrates that the design intentions are reflected in the measured electrical characteristics of the DEPFET. So far the short gate design seems promising because of its low g_m that should result in higher DEPFET gain and lower noise. In addition the clear process should be possible with moderate voltages and faster due to the shorter drift distance between internal gate and clear. But the electrical characterization is not sufficient for a final success evaluation because it cannot determine the dynamic properties of the pixels and their interaction. That is why the pre-characterized detector dies are currently being integrated into full detector systems. Spectroscopic measurements will be performed as proof of principle and it will be studied how the design properties investigated with the electrical characterization translate into the performance of the detector. Only then it will be possible to find the most suitable DEPFET design for the wafer-scale application ATHENA+. In addition device

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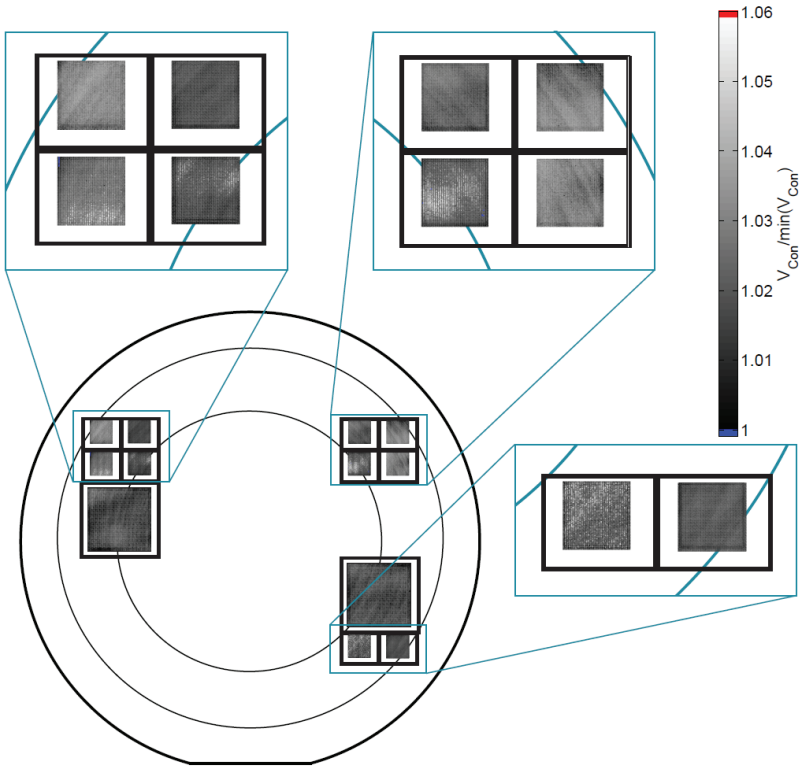

Figure 7. Maps of the onset voltage of the clear V_{Con} for 2 MIXS macropixel matrices and the surrounding 10 ATHENA+ prototypes with respect to their wafer position are shown. Because of the different DEPFET layouts V_{Con} is normalized to the minimum value for every die. A concentric structure is visible for all devices with varying markedness due to the resistivity variation of the high ohmic float zone silicon wafer material [3].

selection criteria for detector integration will be defined. Furthermore the obtained measurement results can be used for simulations of the contribution on noise and achievable readout speed of the device itself in the detector system using SPICE simulators such as Cadence Virtuoso Spectre Circuit Simulator.

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Versicherung

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Filderstadt, den 22.12.2015

Bettina Bergbauer

Theses

1. During several measurement series it was found that the detector gain g_d as well as the charge transconductance g_q do not follow the theoretical expectations deduced from the transistor equations.

2. The suggestion, that g_d is constant for varying gate-source voltages V_GS is not supported by the measurement results of the gate on voltage V_Gon variation.

3. For an increase of the transistor current I_PMOS, the transconductance g_m increases faster than the charge transconductance g_q leading to a decrease of the detector gain g_d.

4. The effective transistor gate area cannot be determined using the design measurements of gate width W and length L.

5. The DEPFET designs are no ideal long channel transistor but complex three-dimensional short channel devices.

6. The presence of short channel effects does not hamper the functionality of the DEPFET but make the clear assignment of measured effects to physical effects difficult if not impossible.

7. The potential drop between source and drain leads to a non-equal distribution of the internal gate underneath the MOS gate.

8. The fraction f of the electrons collected below the transistor channel Q_iG, which induces additional holes in the channel and thus modulate its conductivity, decreases for an increasing transistor current I_PMOS.

9. For short channels the amount of electrons collected in the internal gate Q_iG, which does also induce charge in source and drain, is underestimated.

10. The production reached a high yield for the investigation sensor structures with 70 defect free devices out of 80, which equals one defect in 10 cm^2 chip area. Nevertheless, the yield must be improved to less than one defect per 54 cm^2 in order to get the wafer-scale devices for Athena.

11. For all designs despite the short gate, an increase of the isolator about 30 nm is helpful in order to increases the breakdown voltage between the polysilicon layers.

12. The gate length variation ΔL resulting from the usage of direct wafer lithography is less than 2.3% for all designs other than the short gate design, which shows 3.9%.

13. The results of column and pixel-wise measurements are comparable. Hence, depending on the required degree of detail and the available measurement time, the appropriate measurement set can be chosen.

14. The two step deep n-doping (DN0/2), which is necessary for the formation of the internal gate, was revealed as production weakness because it lowers the potential barrier of the clear contact leading to charge loss.

15. The predictions made by the electrical qualification concerning the detector biasing are found to be useful. For an empty internal gate, the PMOS transistor of the DEPFET behaves for dynamic conditions of the spectroscopic measurements equal as for the quasi-static electrical measurements. In order to ensure a complete clear process under dynamic conditions, a safety margin must be added to the predictions of the quasi-static electrical qualification.

16. When the biasing voltages provided by Athena flight periphery are sufficiently stable, the narrow gate structure is recommended. Otherwise, the quasi linear design is recommended as it is the most stable and shows the largest operation windows for the clear gate off voltage V_{CGoffS} and the clear off voltage V_{CoffS}.

17. Independent of the DEPFET design, the backside voltage V_{B} should range between -110 V and -150 V and the ring voltage V_{R1} between -12 V and -17 V in order to deplete the device fully and form the potential funnel towards the internal gate.

18. An inner substrate bias V_{InS} of +0.3 V is sufficient to drain the surface leakage current from the polysilicon structures of the DEPFET for all design variants.

19. Even with the parallelization of the readout and the signal multiplexing as well as increasing the general sequencing frequency, the required row processing time $t_{\mathrm{Row}} = 2$ µs for Athena cannot be reached with the source follower readout.

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Lebenslauf

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